100MPL MIDI PROGRAMMABLE GUITAR PREAMP
PREAMP CIRCUIT DESCRIPTION

GK Document #: 450-0065-E1
Preamp Board #'s: 206-0065E
Model #'s: 100MPL All Options
Date: 5-10-91

INTRODUCTION

The following is a brief description of the operation of the circuits found in the 100MPL MIDI Programmable Guitar Preamp from Gallien-Krueger. It should provide enough information required to get a basic understanding of the circuits in order to perform any neccessary repairs. When calling attention to a component with the use of a reference designator, the r.d. shown will be that of the E revsion preamp board, PCO 18.

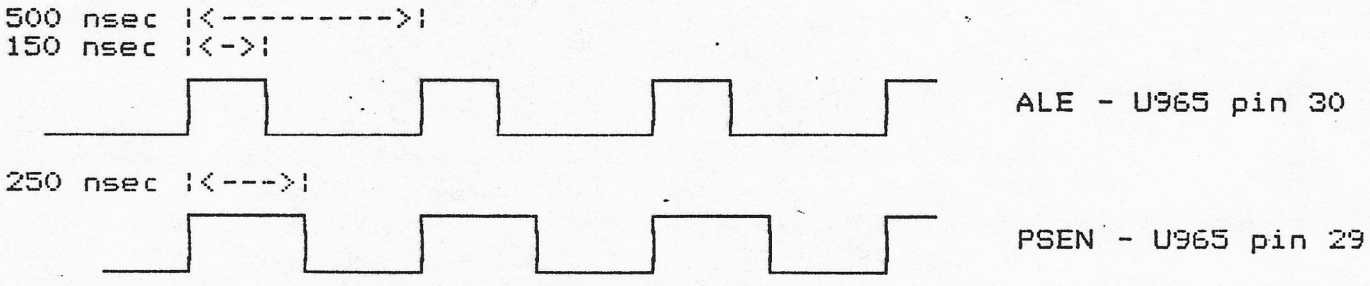
CIRCUIT DESCRIPTION

The 100MPL is a digitally controlled analog signal processor for guitar. All of the adjustable elements in the signal path are controlled either by a DC voltage (for example, Volume), a TTL-level analog switch (channel select), or specially coded pulse trains on several lines (the equalizers). The 8031 microcontroller drives all of the circuitry required to generate these signals as well as storing and recalling these combinations of settings which comprise a patch. The built-in serial port on the 8031 handles all MIDI communication.

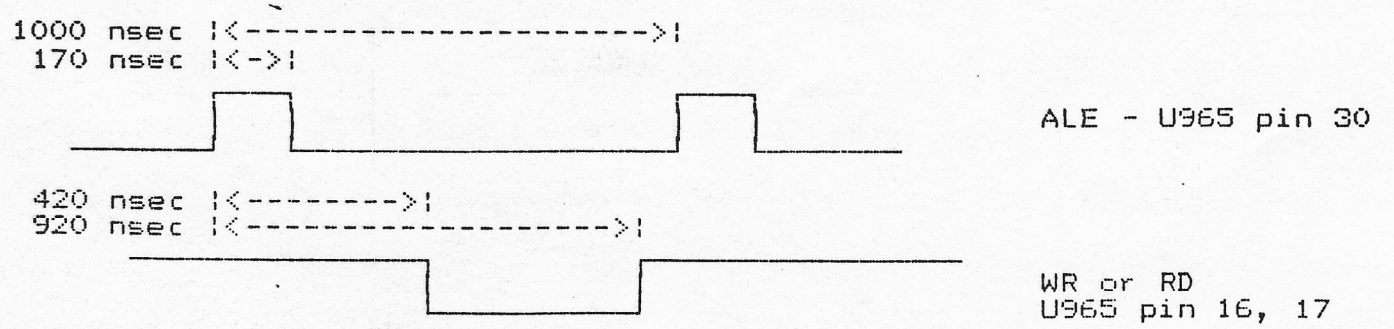
DIGITAL SECTION

The heart of the digital section is the 8031 microcontroller U965, the 27C256 PROM U939 which holds the operating firmware, the 6264-LP low-power CMOS static RAM U937 which holds the patches among other things, and the 74HCT373 octal latch U958 which handles the multiplexed address/data lines on the 8031. In order to use external data memory, pin 31 (Vdd/EA) of the 8031 must be grounded. Pin 30, Address Latch Enable (ALE) latches the low address byte into latch U958 in the early part of the memory cycle. The low part of the address is stable when ALE is low. Pins 32-39 on the 8031 perform double duty as address lines early in the memory cycle, then after the address has been latched, they are used to read instructions and data in or out of the CPU. In normal operation, ALE is a TTL-level rectangular wave with a period of 0.5 usec. Pin 29, Program Store ENable (PSEN), goes low to enable the outputs of the PROM U939 so that the CPU can read an instruction or table entry. PSEN is also a TTL rectangular wave with a 0.5 usec period, but the pulses are slightly wider than ALE.

1) ROM (program instruction) read cycle (WR and RD are both high)



2) RAM (data) read or write cycle (PSEN stays high)



12 MHz crystal Y961 determines the fundamental operating speed of the CPU. The RAM cycle frequency is 1/12th of the crystal frequency. If ALE and PSEN seem dead, check for a 12 MHz oscillation on pin 18 of U965. The amplitude should be about 2V p-p. WR (pin 16) and RD (pin 17) control access to the RAM. These pins normally show a 500-nsec wide low-going TTL pulse that is synchronized with ALE, but at a much slower rate. This is a result of many fewer accesses on the average to RAM versus ROM. The ROM is decoded at addresses 0x0000-0x7FFF. The RAM is decoded at addresses 0xC000-0xDFFF. Note, however, that the instruction bus and data bus are independently accessed, allowing up to 64k of code and 64k of data. This is known as a Harvard architecture CPU, in contrast to the more prevalent Von Neumann architecture where data and program code are accessed by the same control lines and cannot have overlapping addresses (e.g. Z-80).

The static RAM has a lithium-cell backup capability so that settings are remembered even with the power turned off. BT936 is a 3-volt nominal lithium coin cell. When the unit is turned on, the battery voltage is monitored by voltage comparator U917. The reference voltage at pin 10 is derived from the +5 volt supply and is typically between 2.4-2.5 volts. When the battery voltage drops below this threshold, Q929 sources current to the decimal point on the LED display, used as a low-battery indicator. The battery is guaranteed to backup data down to Vcc = 2.0 volts. Diode D942 has a forward drop of about 0.2 volts at the very low current which the RAM uses. This gives 0.2 to 0.3 volts of headroom. The LF347 BiFET op-amp is used to prevent any load on the battery other than the RAM. Transistors Q952 and Q943 and associated resistors handle switching the RAM supply from the +5V supply to the lithium cell. When +5V is available, the divided voltage at Q952's base is adequate to turn it on, drawing current thru R949 and thus Q943's B-E junction. This saturates Q943 and delivers very nearly the full supply voltage to U937's Vcc. When the supply falls, Q952 stops conducting, Q943 turns off, and current begins to flow through D942, which is now forward-biased. Another part of the battery back-up circuit involves Q982 and one gate from U988. The PSOK signal is generated on the power supply board and is high when there are several volts of input headroom on the +5 volt regulator. When the power supply is turned off, this signal gives an advance warning via PSOK, buffered by U988. Normally, when PSOK is high, Q982 passes the chip-select signal presented on its emitter to CS1 of U937. When PSOK goes low, a few moments before +5 volts drops out, Q982 is turned off and CS1 is pulled high through R941. This is a condition which has to be met for data retention to occur properly.

The interface to the 100MPL's signal hardware is provided by five 8-bit latches in 3 separate sections. Latch enables are generated by address decoder U972, a 74HCT238, in conjunction with part of U968 and address lines A1,A2,A3 and A13 from the 8031. The address decoder outputs respond to DATA write and read cycles in the address range 0x2000 to 0x200E on even boundaries. These are the ones that are used:

0x2002 - Display Data
0x2004 - Display Control
0x2006 - Switch Control
0x200A - Digital-to-Analog Convertor (DAC)
0x200C - Control Voltage Multiplexer and Equalizer Interface

U869 at 0x2002 and U856 at 0x2004 handle the interface to the 7-segment LED display and the 2x16 LCD readout on the front panel. U869 latches the data value while U856 handles the clocking signals to both the 4511's (U810 and U833) which drive the LED's and to the LCD module. The LED board (Assy # 206-0069) holds a 2-digit 7-segment readout to display the patch number and four green LED's and current limiting resistors for the clipping indicator circuit.

U851 at 0x2006 provides 8 one-bit controls:

Bit 0: Chorus On/Off (0 = On; 1 = Off)
Bit 1: FX Loop In/Out (0 = In; 1 = Out)
Bit 2: Noise Reduction On/Off (0 = Off; 1 = On)
Bit 3: Input Gain Boost (0 = Off; 1 = On)
Bit 4: Overdrive Select (0 = OD1/2; 1 = OD3/4)
Bit 5: Clean/Overdrive Select (0 = CLN; 1 = OD1-4)
Bit 6: EXT2 drive (D rev boards) EXT1 drive (E rev and later)
Bit 7: EXT1 drive (D rev boards) EXT2 drive (E rev and later)

Control voltages are generated and distributed by U919 at 0x200C (multiplexer control) and U901 at 0x200A. The DAC uses a network of 1% resistors in an R/2R configuration to provide a scaled voltage proportional to the digital code latched in U901. This voltage is amplified and buffered by U900. U900's output goes to the inputs (pin 3) of U883 and U868, both 4051 CMOS analog multiplexers. The address and enable lines (pins 6,9,10, and 11) on the 4051's determine where the current DAC voltage will be routed on the board. Pin 6 of U868 normally shows eight low-going pulses about 40 usec apart, synchronized with the falling edge of the 100 Hz square wave from U989 pin 3. Pin 6 of U883 will show 6 low-going pulses. U918, a Hex open-collector buffer (7407), provides logic level shifting between U919 (+5V) and U883 and U868 (+15V). The outputs of the 4051's go to a series of sample/hold amplifiers (op amps U900, U917, U882, and U867).

The S/H amps keep the control voltage from sagging between updates. Each S/H amplifier control voltage output is further filtered by a simple R/C network before venturing out into the analog section. This helps stop coupled digital interference as well as slowing the control voltages down so that rapid changes in control levels are smoothed out a bit.

Pins 1-8 on U965 form the 8031's parallel port 0. These lines are brought out to connector P970, which connects to the front-panel membrane switch array. The first four lines are pulled up to +5 by 1k resistors and are the Keyboard Sense Lines. They are configured by software as inputs to read external data. Pins 5-8 are configured as outputs, and sequentially drive each Keyboard Drive Line low in order to scan for keypresses. The switches are arranged in a 4 x 4 matrix, giving a maximum of 16 distinct keys. Fourteen of these are on the front panel. The other two are driven by current flowing in Q1003 and Q1002 which connect to the RFP-2 footswitch input. When contact is made, a sense line connects to a drive line and will be pulled low during the scanning period (this happens about 100 times a second). This information goes into the CPU, where all of the keys are debounced. Once a key has debounced (by making contact for several consecutive scans), its code is sent to the operating program.

U989, a 555 timer, provides a 100 Hz rectangle wave which interrupts the CPU via the INT1 line, pin 13. This interrupt is vectored to a routine which scans the front panel and handles the control voltage updating, as well as other tasks.

6N139 optoisolator U969 and two gates from the 74LS09 open-collector quad AND gate U968 comprise the MIDI interface hardware. The optoisolator output responds to current flowing in its input LED (presumably from the MIDI OUT of another device). This signal is sent to RxD (Receive Data) pin 10 of the 8031. It is also buffered and appears at MIDI thru (J16). The MIDI out signal originating at TxD (Transmit Data, pin 11 of the 8031) is also buffered by a 74LS09 gate and appears at MIDI out (J15). Note that since the LS09 is an open-collector device, no signal will appear on the gate output unless the current path is completed (presumably by the MIDI input circuit of another device). The MIDI interface uses an optically isolated current-loop to transfer signals. This avoids direct electrical connection between sending and receiving systems, thereby preventing audio ground loops.

ANALOG SECTION

INPUT STAGE

The input stage is built around J113 JFET Q30. In CLN, OD1, and OD3 voicing modes, the gain of this stage is roughly 4 (12 dB). For OD2 and OD4, JFET Q25 is turned on, effectively bypassing the source through capacitor C28, and the gain goes up to 7 (17 dB). Note that the first attenuator cell, U48, forms part of the AC load on the drain of Q30. The gain of Q30 varies with the impedance of U48 which depends on the GAIN setting. Q30's gain is 5 dB higher when the GAIN is at 50 versus its gain when GAIN is 0 (the above figures were taken with GAIN at 50). With high level input signals, the clipping characteristics change due to shifting of the load line.

VOLTAGE CONTROLLED ATTENUATORS

The channel gain in the lead channel is set by two VTL5C4/2 optically coupled photoresistors, U48 and U449. The clean channel gain is affected only by the first attenuator. These photoresistors are

driven by feedback-controlled opamps (U418) which sense the voltage drop across a 22k resistor connected to +15V on one end, and one end of the attenuator cell on the other. The center tap of the attenuator cell is grounded, so that this sense voltage, which is applied to the non-inverting input, is proportional to the resistance of the cell. When the control voltage is increased at the inverting input, the current being driven through the LED decreases, which makes the voltage divider voltage increase to match the control signal. Therefore, maximum attenuation occurs for a control voltage of zero, and minimum attenuation (maximum gain) occurs when the control voltage is as high as it will go (about 13.5 volts). In any OD mode, both attenuator control voltages are the same. In the clean mode, only attenuator #1 is controlled, and attenuator #2 is set at minimum gain to reduce lead-channel feedthrough to the clean channel.

UNBALANCED DIRECT OUT

Q27 (J113) is configured as a source follower to give a relatively low (12k ohm) impedance signal buffered directly from the instrument input. This signal can be used to drive the input of a guitar amp or multi-effects unit, for example. The gain from the input to the direct output is unity.

LEAD CHANNEL

The overdrive in the lead channel is generated by the high gain of three FET's. Q59 forms the first stage of gain. For OD3 and OD4, Q53 is turned on, which bypasses Q59's source to ground through capacitor C57. In these modes, Q59's gain is about 10 at 100 Hz. For OD1 and OD2, Q53 is turned off, which places the network formed by R56, C55 and R54 in series with C57. This drops Q59's gain at 100 Hz to about 1, and to 4 at around 2 kHz, where it begins to roll off at -12 dB/octave. The result of this is that OD1 and OD2 have less gain than OD3 and OD4, but also have a brighter sound due to the peak in the high midrange. Q59's drain sits at 6.3 V typically. Following Q59 is attenuator #2, as described above. The last two stages of gain are provided by Q457 and Q477. Each of these FET's has a bias trim to set the clipping characteristics, and Q457 has a pot which attenuates its input to allow setting a uniform gain in the lead channel. R450 is adjusted to place Q457's drain at 4.0 to 4.5 volts, and R454 is adjusted to put Q477's drain at 5.8 to 6.2 volts. R455 is adjusted to trim the gain of the lead channel. Each of these FET gain stages should clip smoothly as they are driven with larger input signals, although the clipping will not necessarily be symmetrical. Q477's drain is buffered by source follower Q484 which drives the lead channel shape circuit. The depth of the notch in the shape circuit depends on U502, another VTL5C4/2 optical attenuator. The controlling current in this cell is not part of a feedback circuit, as both halves of the cell are used to control the two independent shape circuits. The lead channel output appears at pin 1 of U503.

CLEAN CHANNEL

The input to the clean channel is at pin 1 of U38, which buffers the output of the first attenuator. This feeds into the variable depth notch ("shape") circuit, whose output is buffered and amplified by two by the other half of U38. This feeds soft clipper/amplifier stage Q453, which has a gain of roughly 20 at 100 Hz. Q453's drain should be around 8.4 volts DC. Unlike the lead channel, the notch is before the clipping stage. With the shape turned up, it is definitely possible to begin clipping Q453. Distortion in the clean channel can usually be controlled by setting the shape at or near zero, and the gain at or below 20. The distortion in this stage should be much less than seen in the lead channel for an equivalent gain.

CHANNEL SWITCHING/VOLUME CONTROL

The lead channel and clean channel outputs are fed to pins 3 and 4, respectively, of TL604 SPDT analog switch U479. The control signal at pin 2 of this chip selects the lead channel with a level of +5 volts, and the clean channel is selected with a level of 0 volts. Output pins 6 and 7 connect to pin 1 of VCA gain cell U498. This point is a virtual ground, therefore no signal will be observed here. The gain of the VCA circuit is determined by the voltage at pin 3. This voltage

has three components, which sum into pin 2 of U480. First is the scaled control voltage CV6. Second is the Voltage trim voltage developed by R486 which allows setting unity gain. Third is the compressor control voltage which comes in through R462.

COMPRESSOR

The compressor is active only when the clean channel is selected. When the lead channel is selected, the compressor control voltages are set such that no compression occurs. The compressor works by automatically adjusting the gain of VCA U498 as the input signal level changes. Clean channel soft clipper output is routed through a precision full-wave rectifier formed by two sections of quad op-amp U419. The output is buffered through diode D422 to C431, which acts as a fast attack/slow release peak detector. When the input level rises, C431 is charged quickly by current sourced from U419 pin 8. When the input level drops, D422 becomes reverse biased, and C431 discharges slowly through R427. This signal level is compared to buffered Sustain voltage CV7 by diode D441. If the peak detector voltage is below the threshold minus one diode drop, the input to the logarithmic amplifier will essentially be the threshold voltage, and no compression occurs. If the peak detector voltage rises above this point, D441 becomes reverse biased, and the log amp input is determined by the peak detector voltage. The log amp output will reflect the changing input amplitude, which automatically adjusts the VCA gain, causing compression.

The use of a log amplifier is dictated by the dBx2155 VCA's control voltage characteristic of -6 mV/dB. To cause limiting, we would have to send a control voltage to U498 pin 3 which increased 6 mV for each dB. Ignoring the effect of Q448, that is essentially the function of the log amp following the peak detector. Q448 and R440 form a voltage divider for the log amp output which appears at U420 pin 14. This scales down the log amp output to give something less than 6 mV/dB, so that the compression ratio is reduced. The amount of reduction is controlled by Q448's drain-source resistance. Since Q448 is being operated with a very small VDS (200 mV max), it functions very well as a voltage controlled resistor. 1 Meg resistors R437 and R443 help to linearize the FET's response. R825 allows trimming the ratio circuit for variations in Q448's Vp. R825 is set so that a ratio of 25 gives full limiting over a 30-dB range. When the ratio is minimum, Q448 is turned on harder, minimizing the corrective effect of the log amp output.

TONE/EQUALIZER

The tone control section of the 100MPL is run by U589, the LMC835 digitally controlled stereo graphic equalizer chip. In this application, it is wired as a four band equalizer with high and low shelving controls, in series with a seven-band equalizer. The response of each band of the equalizer is determined by the resonant frequency and Q (sharpness) of the gyrator sections attached to pins LC1-LC11. Each of these sections behaves electrically like a series L-C network, except the high and low shelving sections, which are a capacitor and simulated inductor (gyrator), respectively. The LMC835 has multiple resistor networks inside which it uses to control the boost or cut of each frequency up to +/- 12 dB. The outputs of the two buffer amplifiers associated with frequency boost (U503 pin 7 and U570 pin 1) are monitored for clipping levels by U809.

The settings of the equalizer are programmed by a specially coded serial bit stream on pins 14, 15, and 16. In operation (i.e., when changing levels on an equalizer band), these pins will be moving between 0 and 5 volts. Being a CMOS part, the LMC835 must operate on reduced +/- 7.5V power supplies. The current needed is so low that this is easily satisfied by zener diodes D591 and D594 and associated parts. The input signal is scaled down by two before entering and scaled up by two upon leaving. For more details on the operation of the equalizer, consult National Semiconductor's Linear Handbook, Volume 3.

NOISE REDUCTION

The noise reduction section is formed by NE572 compander chip U220, along with 5532 low-noise bipolar op-amp U219. They are connected as two VCA's in series. The first VCA is configured with a tracking

voltage controlled conductance cell from the 572 in its feedback network, and the gain control rectifier signal being driven from the input. This results in a VCA whose gain decreases linearly as the input level increases. The second VCA is configured with the tracking conductance cell in its inverting input path, with the gain control rectifier also driven from the input (to the entire noise reduction section). This VCA's gain increases linearly as the input signal increases. If this were all there was, the second VCA's gain would compensate for changes in the first, and the result would be unity gain for all signal levels down to the tracking limits of the 572.

The purpose of the noise reduction is to reduce the gain when the input signal drops below a certain threshold, corresponding to the difference between a sustained note played on a guitar versus the noise and hum that are coupled through in high-gain modes when the guitar is not actually playing. To cause this gain reduction, a DC bias current is injected into the gain-control rectifier input of the first VCA at pin 13. When the input level drops below the point where its contribution to the current at this node is less than the current being supplied through R235 by CV10, the first VCA's gain remains constant, while the second VCA's gain decreases, providing the desired downward expansion. The threshold level is set by CV10, which varies between 3.0 and 5.8 volts DC as the Noise Reduction threshold is adjusted from 0 to 25.

EFFECTS LOOP

The mono effects loop follows the noise reduction output. The signal is scaled down by the R243/R244 voltage divider to present a less hot signal to an effects box input. The level here might still be too hot for some stomp-box type effects which really want an instrument level input. The return signal is protected if need be by zener diodes D242 and D240, and sent to pin 4 of TL604 analog switch U245. The return signal is also sent to the clipping indicator comparator U809. The effect send signal goes to pin 3 of U245, so that the return can be bypassed by applying +5 volts to U245 pin 2. The signal is then boosted again following the analog switch output by half of U655.

STEREO CHORUS

After the Return, the signal goes through an inverting op amp with a gain of 1.5, U655. R302 and C304 pass the low frequencies straight through to the summing amplifier U333. The high frequencies are sent, via the filter of C669, R309 and R310, to the chorus input compressor, U718, and to the chorus select analog switch, U315. The compressor and expander around the chorus circuitry provides for low noise operation. The compressor is built around one half of U718 and is configured to give 2:1 compression. Pins 2, 3, 6 and 7 should all have the 1.8Vdc offset. Pin 1 again has a dc voltage that changes with the level of the input signal. The internal op amp is used in this case so the output is pin 7 and it is biased to 7.2Vdc for operation between gnd and +15V. This goes into a 2-pole lowpass filter, with a cutoff at 3.6kHz, built around U717. The 1N747 diodes limit the signal so that it doesn't overload the Bucket Brigade Delay chip, U678. The center position of the trimpot R676 is generally an acceptable dc bias setting of around 6.3Vdc at U678-3, but if the output of U678 appears to be distorting early on one side it can be adjusted to eliminate that problem. The MN3101, U679, takes a single, 0-to-15V, square wave clock pulse from a 4046 CMOS PLL (we only use the VCO section), U657, and generates the two, out-of-phase, clock pulses used by the BBD for its sampling. These square wave signals are 0 to 15V and have a period that varies roughly between of 20 (DLY = 50) to 70 microseconds (DLY = 0) (with depth at 0). Control voltage CV9 controls the frequency of the 4046 VCO. After the signal has been sampled, the delayed version appears at pins 7 & 8 of U678. The two signals are summed together through R687 and R690 and then must be low pass filtered to remove the sampling frequency element. It then passes through a 5-pole filter, built around U719, that has a cutoff frequency, like the chorus input filter, of 3.6kHz. Finally, it reaches the output expander that "undoes" what the input compressor did and expands the dynamic range back to that of the original input signal. The expander circuit is built around the other half of U718 and uses an external op amp, U717. It also has the 1.8Vdc level at pins 11, 12, 14, and 15 and at U171-5 & 6. The output, U717-7, should be at 4.0Vdc. And again, U718-16 has a dc voltage that varies with the incoming signal level. At this point, the high frequency

(above 3.6kHz) components are added back in using the high pass filter of C730 & R737 and the summing resistor, R733. This signal then goes to U717-6. When U315-2 is +5V (Chorus "OFF"), the dry signal going to pin 3 is selected and the chorus is off. If the Chorus parameter is set to "TRI" or "RND", the voltage on U315-2 becomes 0Vdc and the chorused signal going to pin 4 is selected. The output of U315 (pins 6&7) is summed in at U333.

STEREO EFFECTS RETURNS (AUX1 and AUX2)

Two adjustable level stereo effects returns are provided by a TDA1074A dual DC-controlled potentiometer U164. This chip runs off a single supply, so it generates its own internal reference voltage at 7.5 volts (pin 8). All of the potentiometer pins (2, 3, 4, 5, 6, 7, 12, 13, 14, 15, 16, and 17) should be within half a volt of this point. The signals enter the attenuator circuit and the outputs go directly to the stereo output mixers (U333). Although control voltages CV3 and CV12 are filtered near the DAC section, additional filtering is provided by C155 and C170 near U164 to prevent rapid control voltage changes from creating audible thumps.

VCV CIRCUIT

The VCV filters built around U720 modify the straight guitar signal by boosting the bass somewhat and rolling off at -12 dB/octave above 3.5 kHz to simulate the "miked speaker cabinet" sound. The VCV input comes directly from the stereo output mixers U333. The VCV output goes directly to the balanced out drivers U108 as well as to a switch on the headphone board so that the input to the master volume control can be selected to come from the VCV. This switch selects the signal going to the headphone amp and the stereo line out jacks J2 and J4. The balanced outs are driven directly from the VCV filter outputs (U720-1 and U720-7) and are not affected by the master volume knob.

TURN-ON/OFF POP SUPPRESSION

Transients at the line outs which occur during power on and off are suppressed by J113 FETs Q327 and Q324. During turn on, C335 charges towards -15 volts through R334, with a time constant of about 7 seconds. The FETS are turned on until Vgs(off) is reached, which has quite a wide range (-0.5 to -3.0 volts). It should be about a second. When the unit is shut off, the end of C342 connected to the +15 volts supply goes to ground. Since C342 was charging through D338 while the power was on, its negative end now has a negative voltage on it which turns on Q332 (A56). This brings the gate voltage to 0 again, turning on the FETs and clamping the line out signal to ground.

SUMMING AMPS

The summing amplifiers built around U333 bring together the dry, chorus, reverb and auxiliary signals to be sent to the power amp. The signal at U333-7 contains a 4:1 mix of chorus to dry signal (when chorus is on) and U333-1 has the opposite mix of 1:4. The signal from U333-7 goes to the left channel VCV, and to connector P998 which links to headphone amp board 206-0070. The signal from U333-1 goes to the right channel VCV, and also is routed to P998. Also mixed in at U333 are the attenuated signals from the Stereo Aux Ins with the tip mixing in at U333-7 and the ring at U333-1.

BALANCED OUTPUTS

The signals from the VCV filters U720 are sent to balanced outputs so they can be used for recording or going direct without miking in a live situation. The signal appearing at pin 2 of each of the balanced outputs, P2 and P4, is in phase with the VCV output. The signal going to pin 3 passes through an inverting, unity gain op amp, U108 so that it is 180 degrees out of phase with pin 2. When the Stereo/Mono switch, S3, is out, Balanced Out Right, P2, carries the signal from U720-7 and Balanced Out Left is the same as U720-1. When S3 is pushed in, however, P2 carries the in-phase signal from U720-7 and the out-of-phase signal from U720-1. P4 then carries just the opposite signals. This gives a mono signal when pins 2 & 3 get mixed together at the board.

CLIPPING INDICATORS

U809, a LM324 quad op-amp, is configured as four voltage comparators to look at positive going peak signals at certain critical points in the circuit path. The output of volume control U480-7, boost sections in the tone control and graphic equalizer at U503-7 and U570-1, and the effects return signal at U245-4, are all monitored by simple voltage comparator circuits. When the signal level exceeds the reference set by the resistive voltage divider, the output of the op amp goes high, turning on the LED in the front panel.

HEADPHONE AMPLIFIER ASSY # 206-0070

The headphone amplifier board is connected to the motherboard by a short 10-wire ribbon cable which provides power and signal paths. The level at the output of the Headphone jack J130 is controlled by the Master Volume knob. U108 and U109 are LM386 chips and can provide about 1/4 Watt each into headphones of 8 ohms minimum. The chips run off of ground and -15Vdc so there is a dc voltage of about -7V on pin 5 of each. The LM386's also have a gain of about 20 so the resistor dividers of R101/R103 and R100/R102 provide attenuation of the signal from the Output Level. VCV switch S127 selects which signal will be routed to the Master Volume Pot R124. When pressed in, the VCV filter outputs at pins 9 and 10 are selected. When out, the Mixer outputs at pins 7 and 8 are selected instead. All of these signals are AC-coupled and referenced to ground by 47k resistors R122, R123, R125, R126 to prevent pops when switching. The Master Volume pot wiper is also routed back to the motherboard where it provides the input signal for the Line Out driver U309.

MIDI PROGRAMMABLE LEAD PREAMP, TURN-ON PROCEDURE

GK Document #: 420-0065-E
Board #: 206-0065, Rev D & E
Model #: 100MPL
Date: 8-06-91

Resistance Loads OFF
Speaker Load OFF
Stereo Y-Cord from Stereo Line Out (J8) to switch box inputs A & B.
Orange end goes to A. Grey end goes to B.
Oscillator: 100 Hz Sine Wave, +4 dBV
Voltmeter: DC volts, 20V range
Scope on CHOP
A: 5V/div, AC coupled connected to AC voltmeter.
B: 5V/div, DC coupled connected to DVM.
Time Base: 2 msec/div

VCV switch OUT
Master Volume All the way up!
Stereo/Mono Switch S9 OUT
Stereo/Mono Switch S3 OUT

NOTE: Where Patch parameters are indicated, only those parameters that are relevant to the particular test are listed. If you are setting up these Patches manually, all of them should have the TREMOLO DEPTH (under the second EFFECTS window) set to 0. The figures referenced are part of the quick test procedure (423-0065-E). The figures are numbered to correspond to the test patch number used, rather than in sequence, which is why several seem to be missing.

1) Follow power supply turn-on procedure. Connect the ribbon cable from the power supply to the motherboard.

2) Turn on the power switch. The LCD display backlight should come on (a dim green light). If it doesn't, immediately turn the unit off and recheck the connections to the LCD. The 2-digit LED should also light up at this point with some random number (probably 15). If it doesn't, turn off the power and recheck the connections to the LED display board. Measure the DC voltage at pins 8 (14.75 to 15.25V) and pin 4 (-14.75 to -15.25V) of U720 (LF353). Measure the DC voltage at pin 40 of U965 (8031). This should be in the range 4.75-5.25 V.

3) Assuming that there were no problems, the LCD display should read "MEMORY BACKUP FAILURE!". If the LCD backlight comes on and the LED lights up but no message appears on the LCD, there is a problem in the digital section.

4) Measure the DC voltage on the lithium coin cell (BT936). It should be at least 3.0 Volts. If it is less than 3.0 volts, replace it with a new battery (094-0068-0).

5) <u>DOWNLOAD TEST PATCHES TO 100MPL UNDER TEST</u> Hold down the "RECALL" and "STORE" buttons firmly while powering up the unit. When the turn-on message appears (Gallien-Krueger 100MPL, etc.), the test patches are loaded in. If in the next step, the patches aren't there, try again. There may be a problem with the membrane switch as well.

6) Set R37.
Oscillator: +4 dBV 100 Hz sine wave.
Plug oscillator output into preamp input jack. On the TEST unit, press "RECALL","0" (NAME/SPECIAL), then "> YES". The LED should display "00", and the upper line of the LCD display should read "Set R37". Look at the signal at TP1, on the near lead of R43, 12K. Adjust R37 for equal clipping on both peaks (see Figure 0). The signal level should be about 15 volts p-p centered around -1 volt DC. Look at the tip of J1, DIRECT OUT. Should see sine wave, about 4 volts p-p.

Patch 00: VOICE:OD2 GAIN:20

7) Set R450.
Oscillator: -66 dBV 100 Hz sine wave.
Measure DC voltage at near end of R464, 2.2k. Adjust R450 so that this voltage is in the range 4.0 to 4.5 volts DC.

8) Set R454.
Measure DC voltage at far end of C478 (223). Adjust R454 so that this voltage is in the range 5.8 to 6.2 volts DC.

Note: R450 and R454 interact! Double check the voltages after step 8 and readjust them until they are both correct.

9) Set R455.
Set DVM for AC RMS volts, 20V range, or use AC voltmeter on 10V range. Press "^" once to access Patch 01, "Set R455". Measure AC voltage at TP6,the near end of C463. Adjust R455 for 1.9 +/- 0.1 VAC at this point.

Patch 01: VOICE:OD4 GAIN:50 SHAPE:25 VOL:40

10) Set VOLUME TRIM R486.
Press "^" once to access Patch 02, "VOLUME TRIM". Turn R486 all th way CCW. All of the clipping lights on the front panel should be on. Turn R486 all the way CW. The clipping lights should all go off. Measure the signal at TP7, the far end of C489. Adjust R486 for 1.9 +/- 0.1 VAC at this point (try to match the voltage set in step 9).

Patch 02: VOICE:OD4 GAIN:50 SHAPE:25 VOL:99

11) Set Up and Test Compressor.
Oscillator: -46 dBV 100 Hz sine wave.
Master Volume Up Full.

a) Press "^" once to access Patch 03, "Set R825". Turn R825 CW until it stops. Slowly turn R825 CCW while watching the level of the output signal. As R825 rotates, the signal will peak slightly, then start to decrease in level. Set R825 at the point where the signal just starts to decrease.

b) Increase the input signal level to -16 dBV. The output (measured at LINE OUT) should stay about the same, although the signal will be distorted. Now decrease the level to -46 dBV, noting that the output level takes several seconds to increase to its previous level. This confirms proper operation of the compressor. There should be no unusual effects such as oscillation during this step.

Patch 02: VOICE:CLN GAIN:50 SHAPE:25 VOL:99 RATIO:25 SUS:25

12) Lead Channel Shape Control and Gain Switching Circuits.
Oscillator: -46 dBV, 100 Hz sine wave.
Press "^" once to access Patch 04, "Lead Channel". Verify that the waveform is similar to Fig. 4 of the scope photos. Press "^" again to access Patch 05, "Lead Shape". Verify that the waveform is similar to figure 5.

Fig. 2: Patch 04: VOICE:OD4 GAIN:50 SHAPE:25 VOL:90
Fig. 3: Patch 05: VOICE:OD4 GAIN:50 SHAPE:0 VOL:90

Check the lead channel switching circuits. Press "^" once for each of figures 6-8, and verify the waveform against the photographs. After Patch 6, increase the oscillator level to -26 dBV.

Fig. 6: Patch 06 (OD3 test) : VOICE:OD3 GAIN:50 SHAPE:0 VOL:90

Oscillator: -26 dBV, 100 Hz sine wave.

Fig. 7: Patch 07 (OD2 test) : VOICE:OD2 GAIN:50 SHAPE:0 VOL:90
Fig. 8: Patch 08 (OD1 test) : VOICE:OD1 GAIN:50 SHAPE:0 VOL:90

13) Check clean channel shape control.
Oscillator:-36 dBV, 100 Hz square wave.
Press "^" once to access Patch 9, "Clean Shape". Verify that the waveform is similar to Figure 9. Press "^" again to access Patch 10, "Clean Chan". Verify that the waveform is similar to Fig. 10.

Fig. 8: Patch 09 (Clean Shape): VOICE:CLN GAIN:50 SHAPE:0 VOL:90
Fig. 9: Patch 10 (Clean Chan): VOICE:CLN GAIN:50 SHAPE:25 VOL:90

14) Equalizer Test
Oscillator: -36 dBV, 100 Hz square wave
Press "^" to recall Patch 11, "EQ FLAT". Verify the waveform against Fig. 11. To check all of the equalizer bands, press "^" for each of figures 12-33, and verify the waveform against the scope photo.

NOTE: before testing Patch 16, "EQ HIMID +12", set the oscillator to 1 kHz, and the scope sweep to 200 usec/div. Before testing Patch 26, "GR 640 +12", set the oscillator to 100 Hz and the scope sweep to 2 msec/div 640 +12", set the oscillator to 100 Hz and the scope sweep to 2 msec/div

Patches 12-33: VOICE:CLN VOL:80 GAIN:50 SHAPE:25 RATIO:0 SUS:0
Each Patch sets a band of the equalizer alternately to +12 dB, then -12 dB to check the equalizer operation.

15) Noise Reduction Test
Oscillator: -66 dBV, 100 Hz sine wave.
DVM on AC volts, 2 volt range.

Press "^" twice to access patch 35, "Noise Red 2". Check that the signal at the output is a clean sine wave (Figure 35). Disconnect oscillator. Connect headphones. Press "v" to access Patch 34, "Noise Red 1". Should hear noise and a small amount of hum. Make sure that both sides of the headphones have the same level coming out. If there is a problem, see step 21, Headphone Test. Noise voltage at output should be less than 55 mVrms. If hum is excessive, check grounding of rear panel to main chassis. Step up through patch 37. The noise and hum should decrease at each step. The noise quality should be smooth, not "crackling".

Basic setting for noise reduction tests:
VOICE:OD4 GAIN:50 SHAPE:25 All equalizer bands set to 0 dB (flat).

Patch 34: VOL:60 NR:ON THRESH:25
Patch 35: VOL:60 NR:ON THRESH:0
Patch 36: VOL:70 NR:ON THRESH:25
Patch 37: VOL:70 NR:ON THRESH:0
Patch 38: not used
Patch 39: not used

16) Chorus Test.
Oscillator: -16 dBV, 100 Hz square wave.
Insert Oscillator output into effects return jack J10.
Scope Channel B: 2V/div. 2 msec/div
Press "^" to access Patch 42, "Chorus Sweep". Look at the waveform at the output. As you adjust R676, notice that at one extreme the top peak of the waveform flattens out (Fig. 42a), while at the other end the peaks disappear. Set R676 at the point where the peak has just regained its pointy shape (Fig. 42b). During this test, the spikes in the waveform will move slowly back and forth.

Patch 42: CHOR:TRI DLY:15 RATE:5 DEPTH:35 Effect Loop:IN

17) Balanced Out/Line Out Test.
Scope Channel A to 5V/div.
Look at the signals on the center and left pins of XLR jacks P2 and P4. Verify that the signals correspond to the proper scope photo depending on the position of the STEREO/MONO switch S3 (see Table 1). Looking at line outputs A & B, check operation of switch S9. When S9 is IN, the waveforms should be identical. With S9 out, output "A" will have a larger peak than "B".

Table 1: Balanced Out Signals

Jack/Pin	S3	Figure
P2 left	OUT/IN	42e
P2 center	OUT	42e
P2 center	IN	42d
P4 left	OUT	42d
P4 left	IN	42e
P4 center	OUT/IN	42d

18) Effects Loop and VCV test
Make sure that the master volume is turned all the way up and that the VCV switch is OUT. Press "^" to access Patch 43, "Loop Enable". Verify the waveforms against Figure 43a. Press the VCV switch IN. Verify the waveforms against 43b. (Check both channels). Vary the master volume over its range to see that the output goes to zero when turned all the way down. Now press "^" to access Patch 44, "Loop Bypass". The output should go to zero, since this Patch bypasses the effect return.

Patch 43: CHOR:OFF Effect Loop:OUT AUX1:0 AUX2:0
Patch 44: CHOR:OFF Effect Loop:IN AUX1:0 AUX2:0

19) Stereo AUX Returns test.
Oscillator: -6 dBV, 100 Hz square wave.
VCV Switch OUT. S9 OUT. Master Volume Up Full.
Plug the oscillator output into AUX1 return J7. You should notice no level coming out at this point. Press "^" once to select Patch 45, "AUX test". Select output "A". The signal at the LINE OUT should look like Fig. 45. Now press "v" (DOWN arrow) to select Patch 44 again. The output should go back to zero. Now slide the oscillator output plug halfway out so that it is contacting the ring of the AUX1 input. Select output "B". Press "^" again to access patch 45. Verify the signal against Fig. 45. Repeat this procedure with the AUX2 input jack J8.

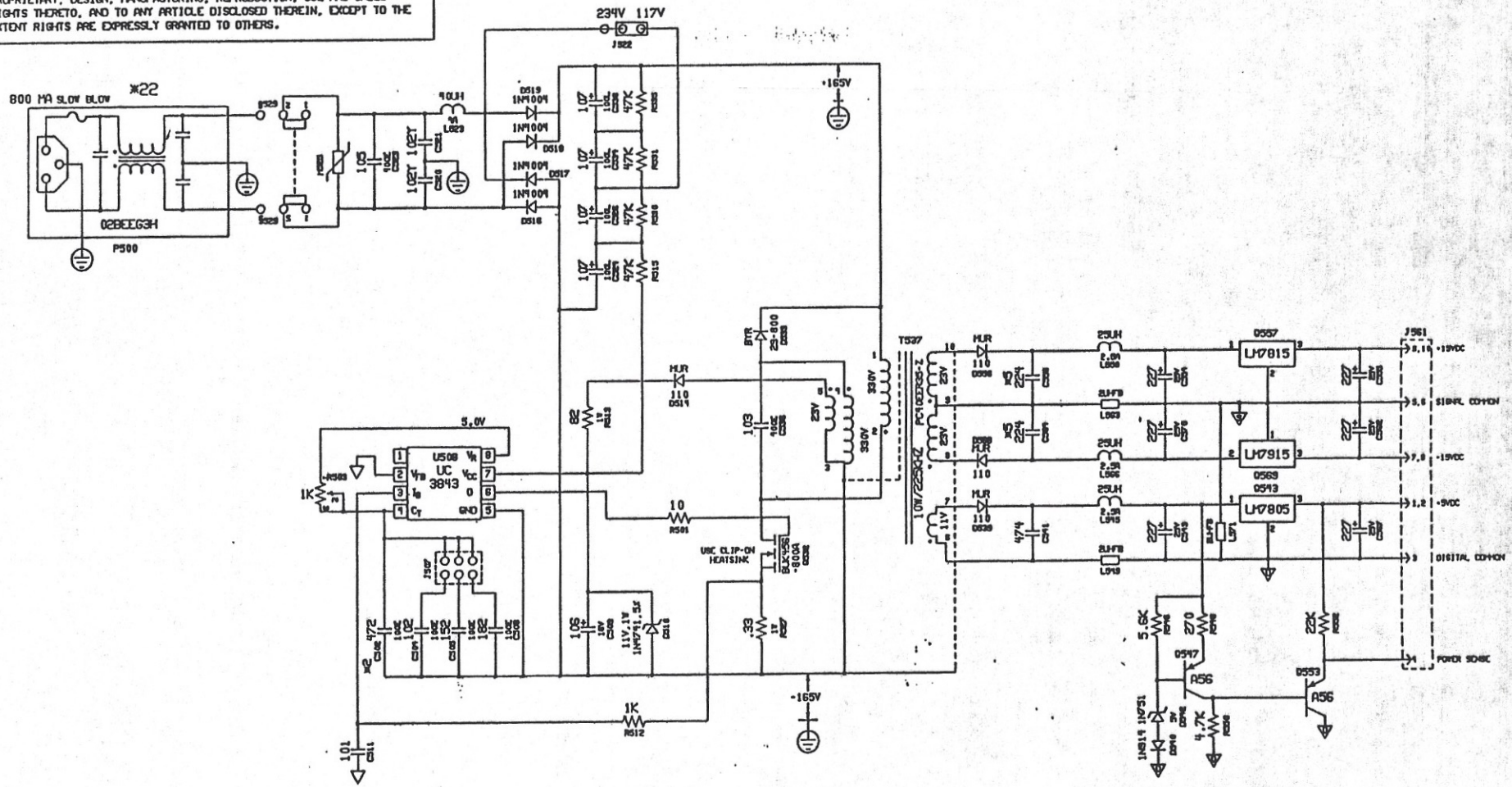
Patch 45: AUX1:50 AUX2:50

20) EXT outputs and phantom power loop
Use 100MPL Test Footswitch.
Plug the 100MPL CNTL TST box into jacks J12 and J13, with the switch and LED's facing up.Plug the 7-pin MIDI plug into the 100MPL's MIDI IN (J17). Insert the proper AC adapter voltage into the Phantom Power Jack (J14). Slide the switch up three times to step through presets 46-48. Slide the switch down to step back down. Make sure that the patch increments and decrements properly. If the patch numbers seem random, check that the "FOOTSW" parameter (under the SPECIAL window) is set to INC. Note that the right, then left, then both LED's come on in the Test Footswitch.

Patch 46: EXT1:+A EXT2:-A
Patch 47: EXT1:-A EXT2:+A
Patch 48: EXT1:+A EXT2:+A

21) Headphone Test. (If problem occurs during noise reduction test).
Oscillator: -16 dBV, 100 Hz square wave, plugged into FX return J10.
Plug stereo Y-cable into headphones jack on front panel.

Turn on power supply and verify that the unit is still working (check display). Recall Patch 42, "Chorus Sweep". Verify that both sides of the headphone amp are working properly. Switch the speaker load alternately to each side, noticing that the chorus sound appears stronger in one channel. The headphone output should clip at around +/- 7.5 volts.



603.0005.4.10

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5	3-25-91		22	7-25-91							

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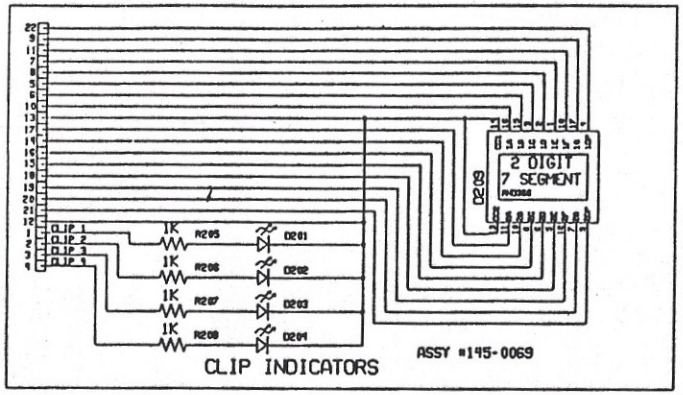

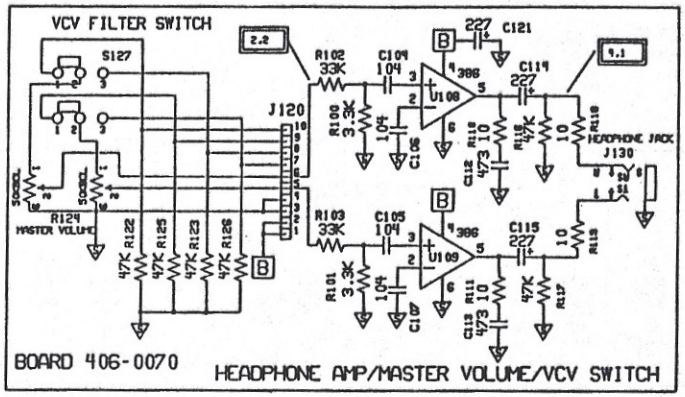

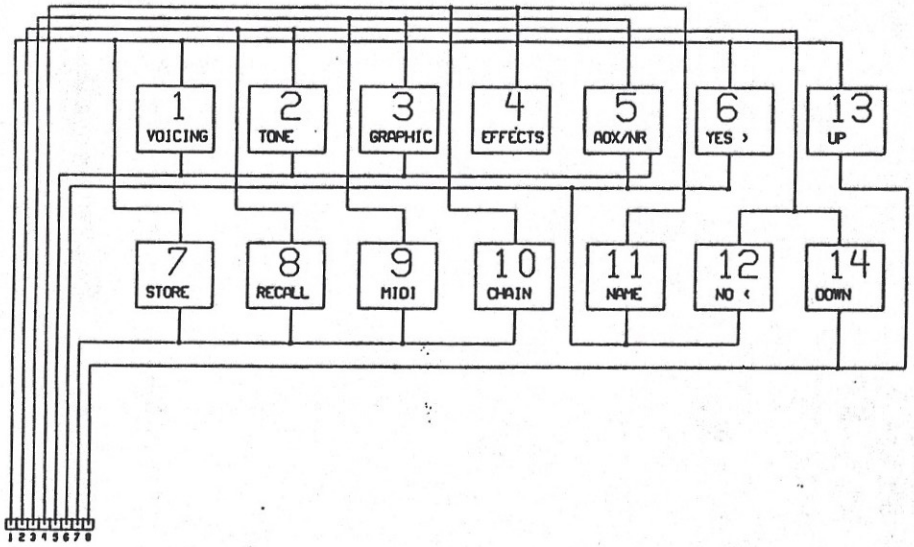

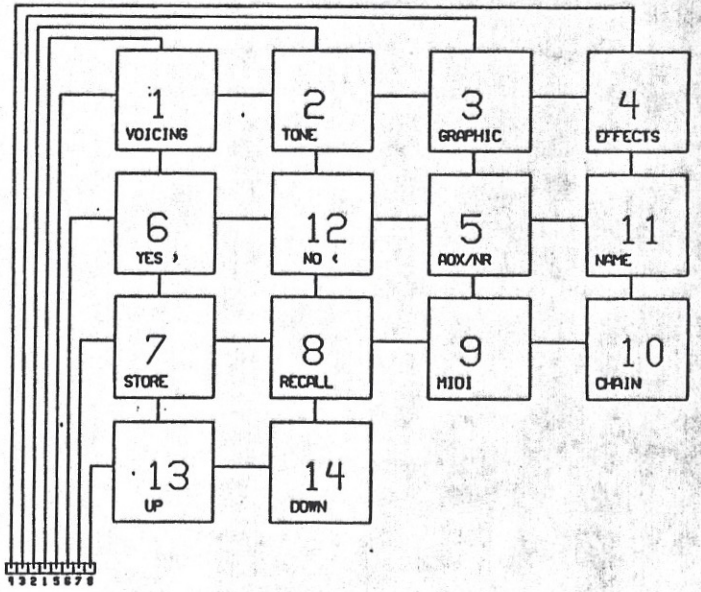

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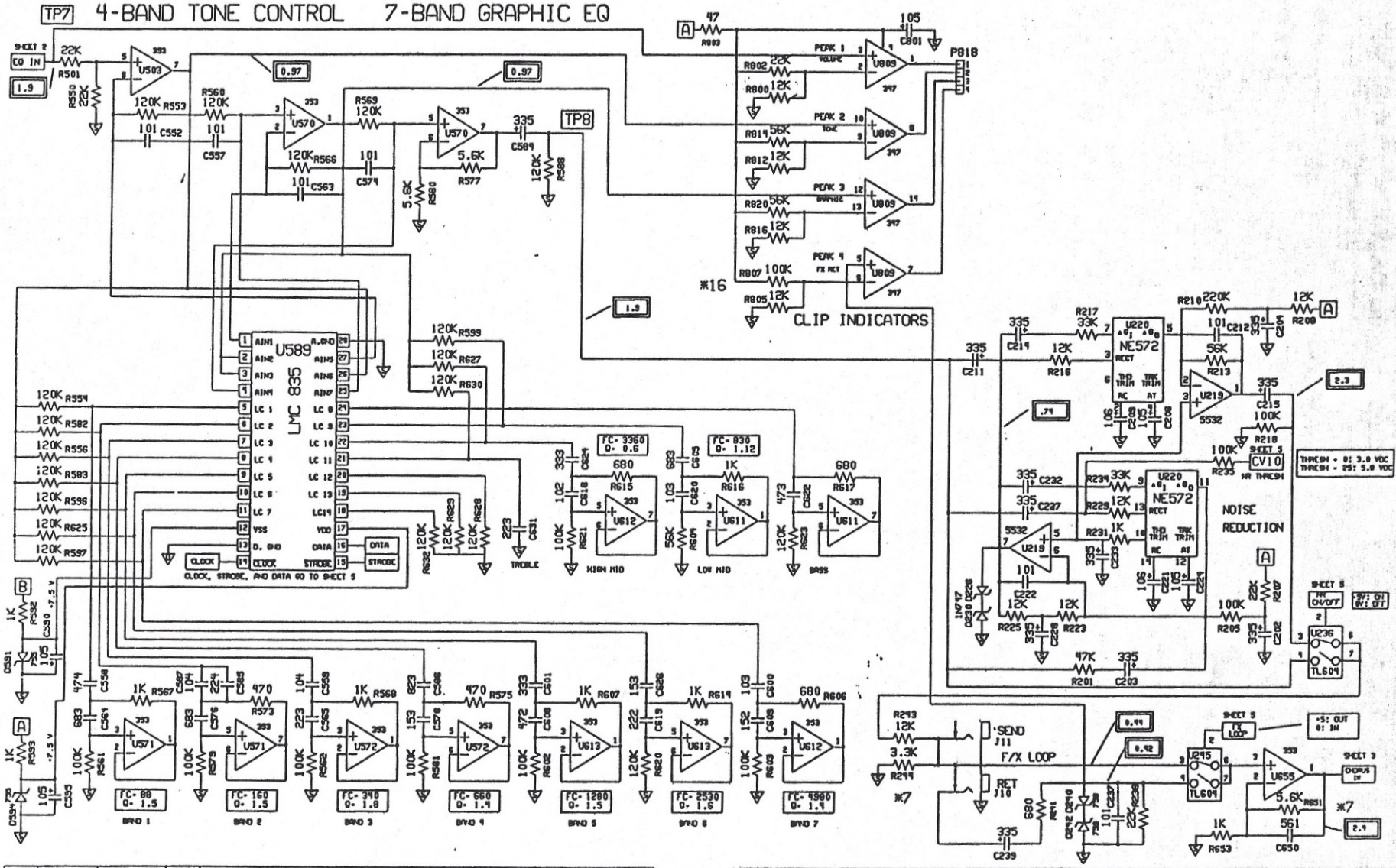

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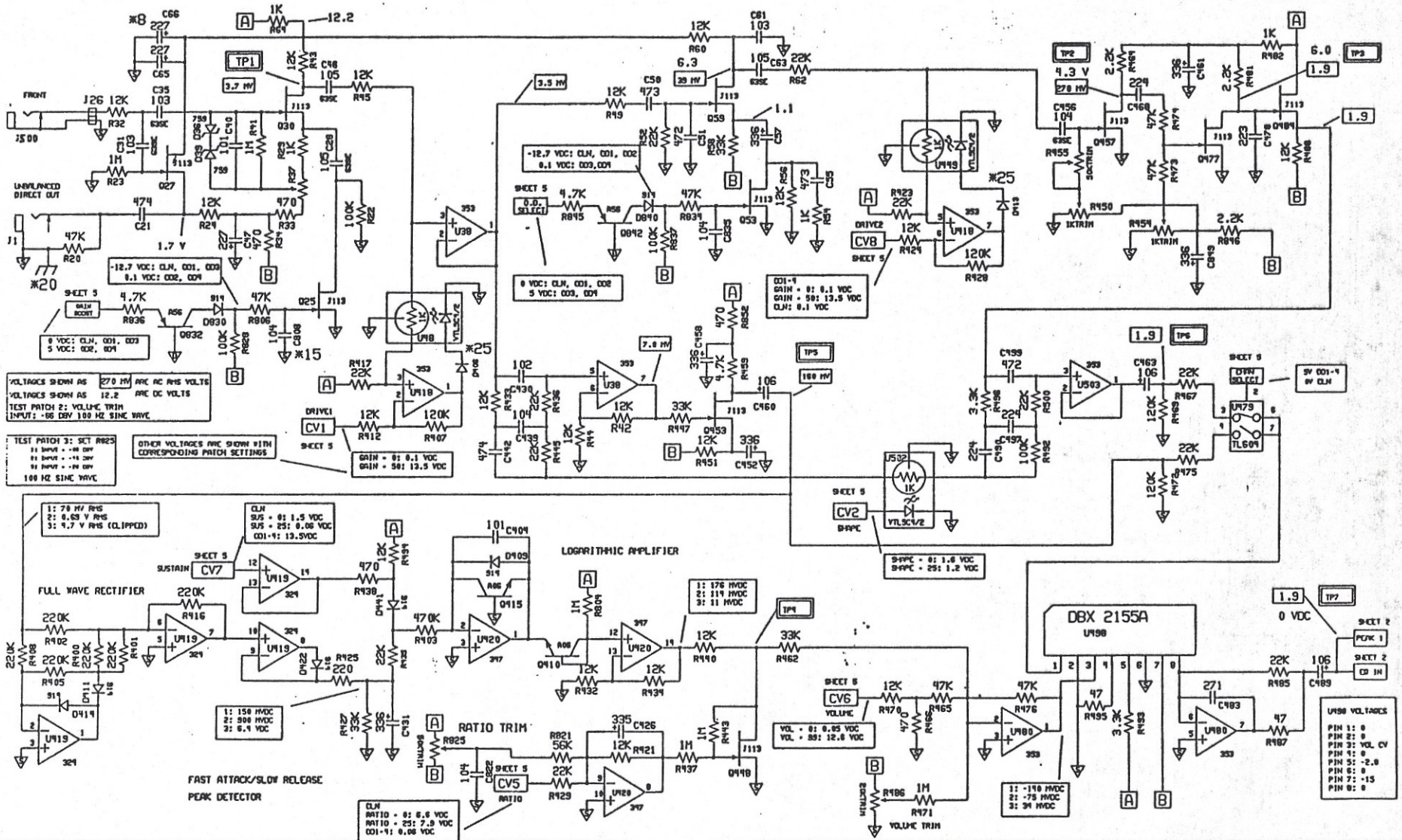
SCHEMATIC PG: 2 OF: 5	DBF: 6006502	DESIGNED BY: G.S.W.	BOARD #: 406-0065D	PCO#-DATE: -	FROM SN:	TO SN:

603.0005.4.31



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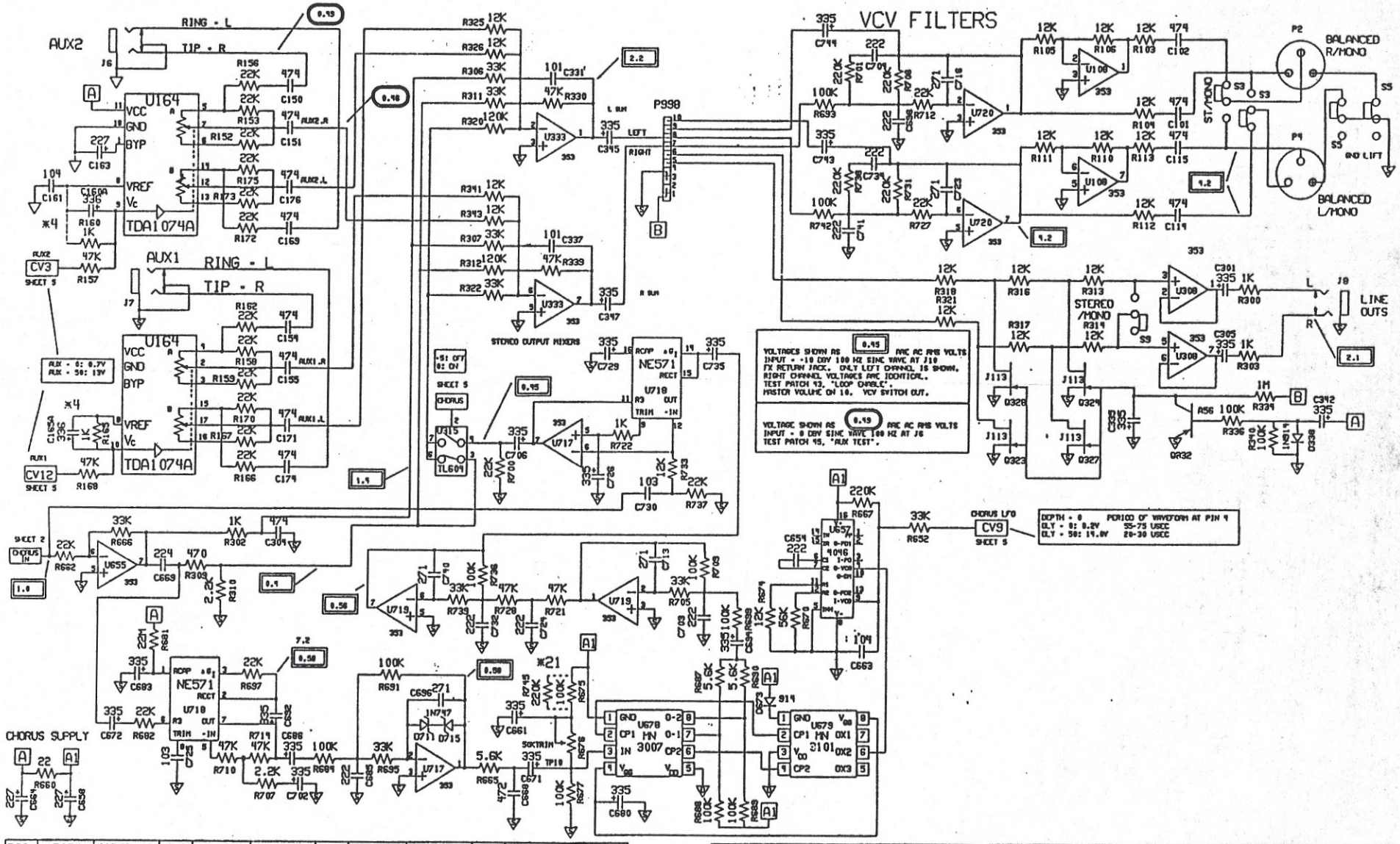

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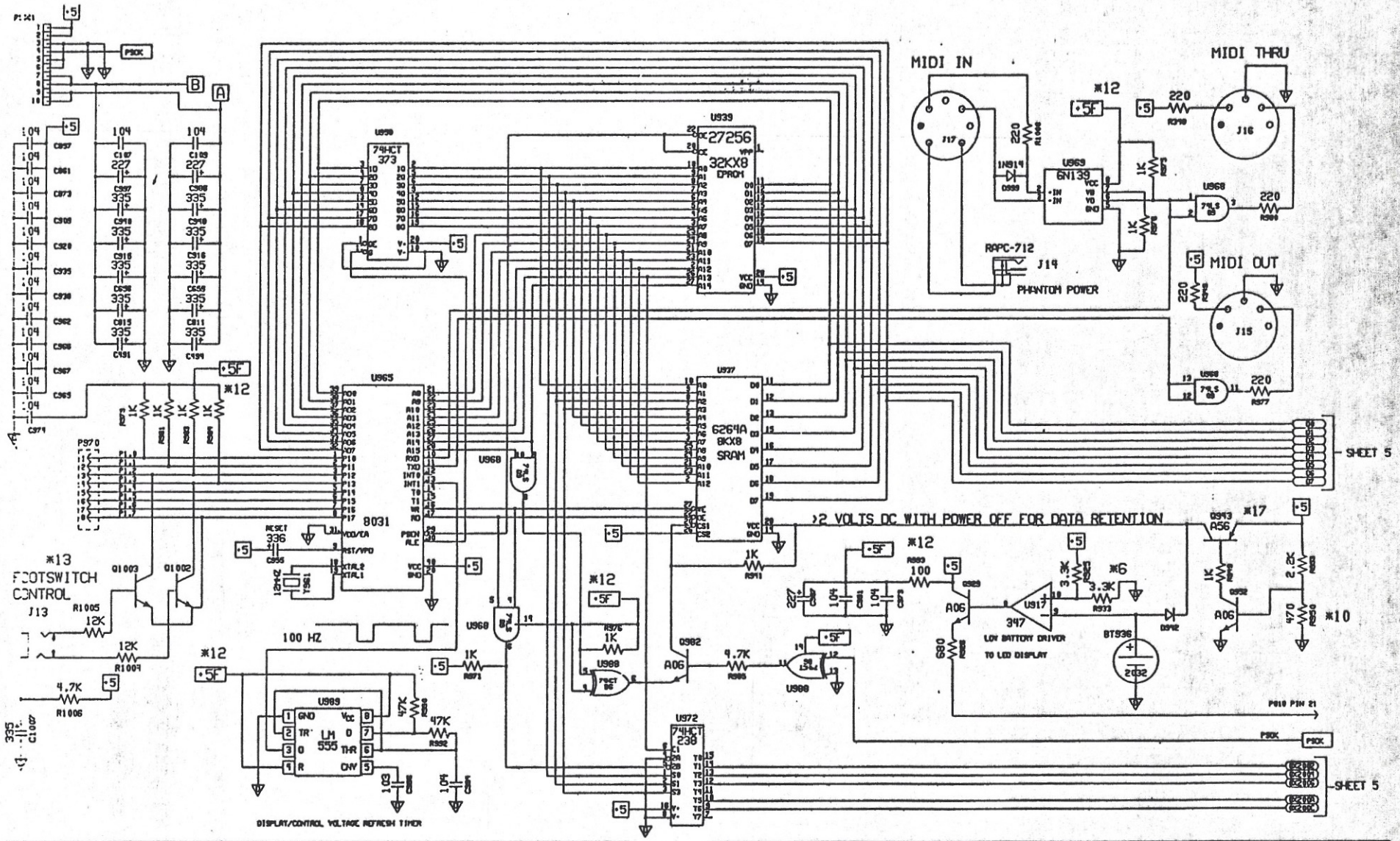

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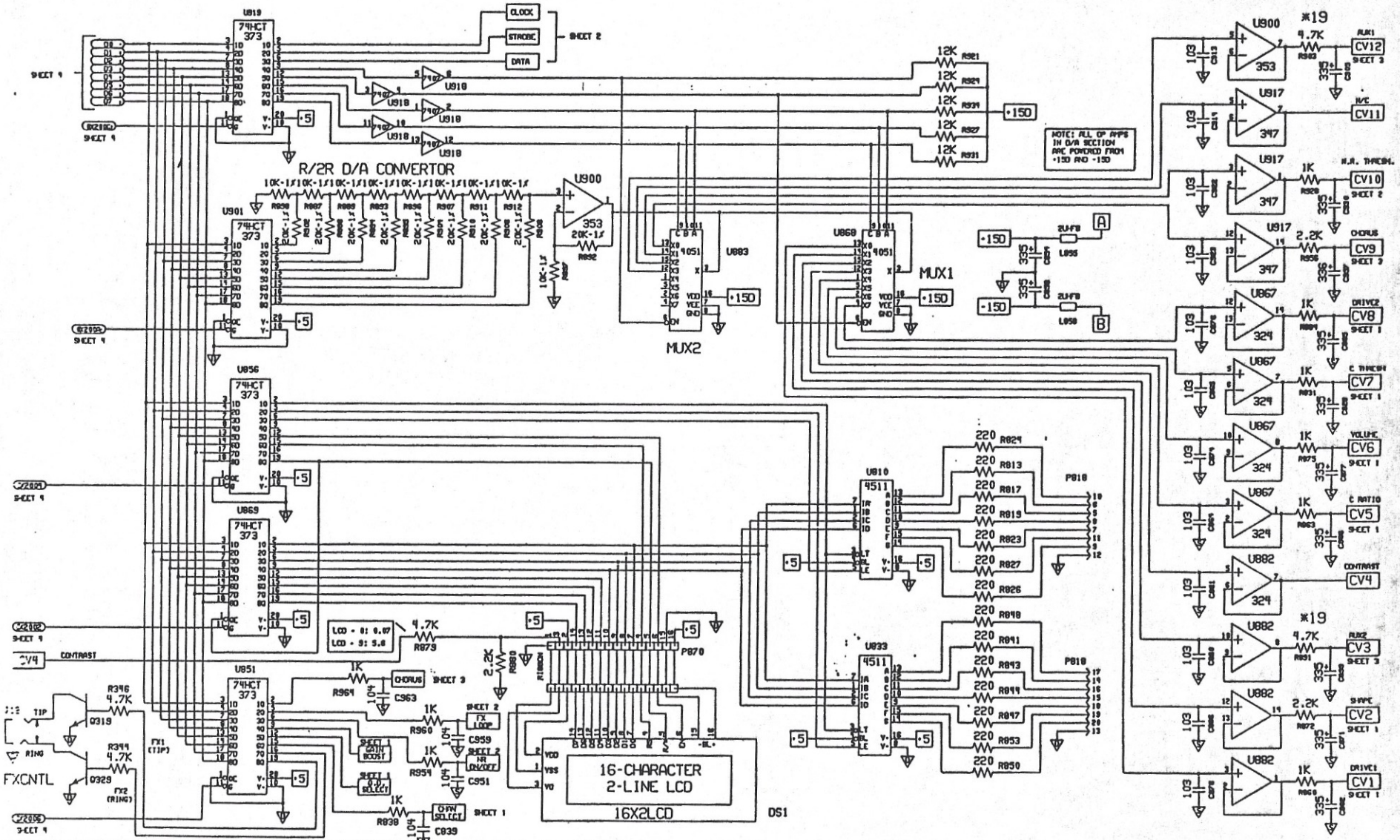

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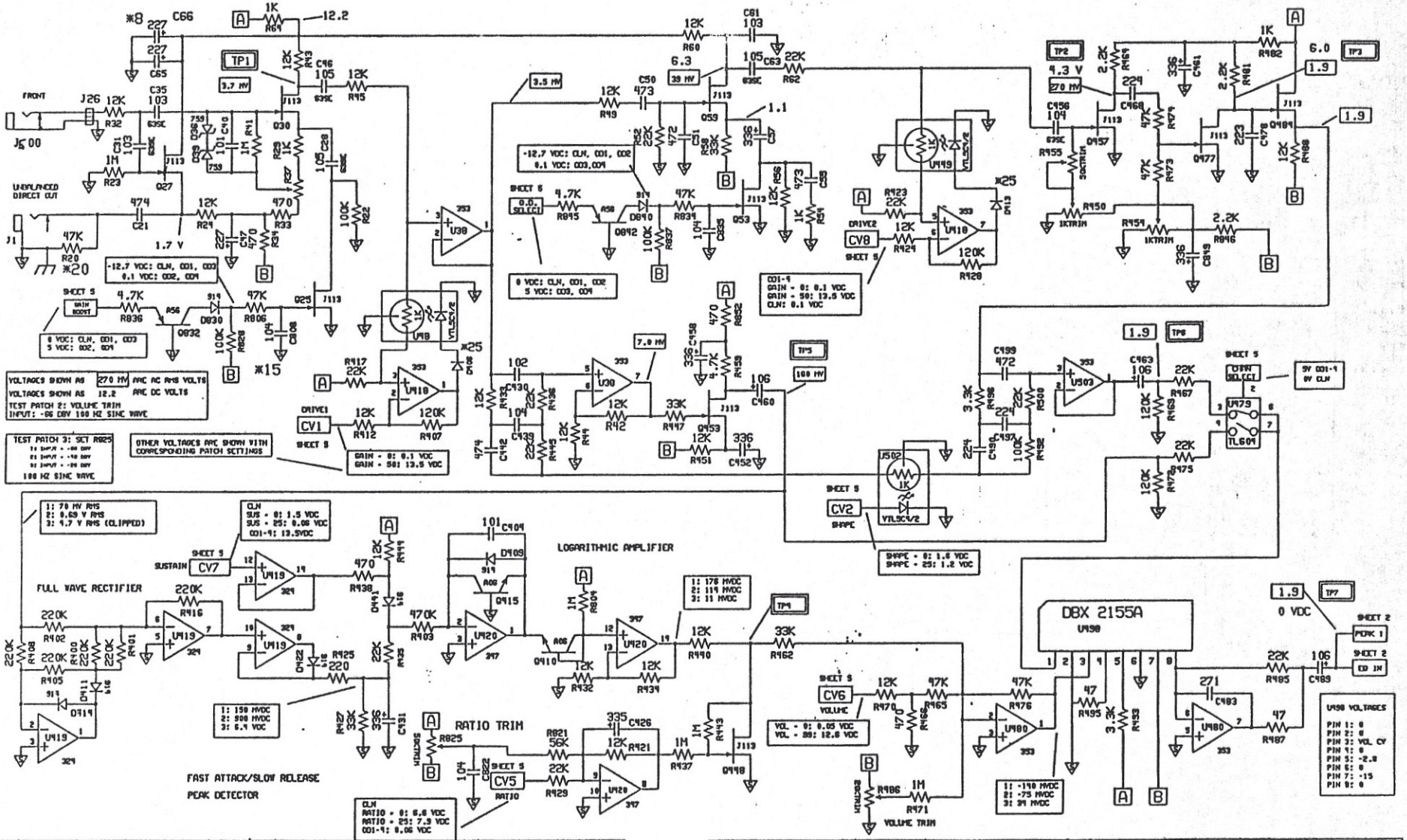

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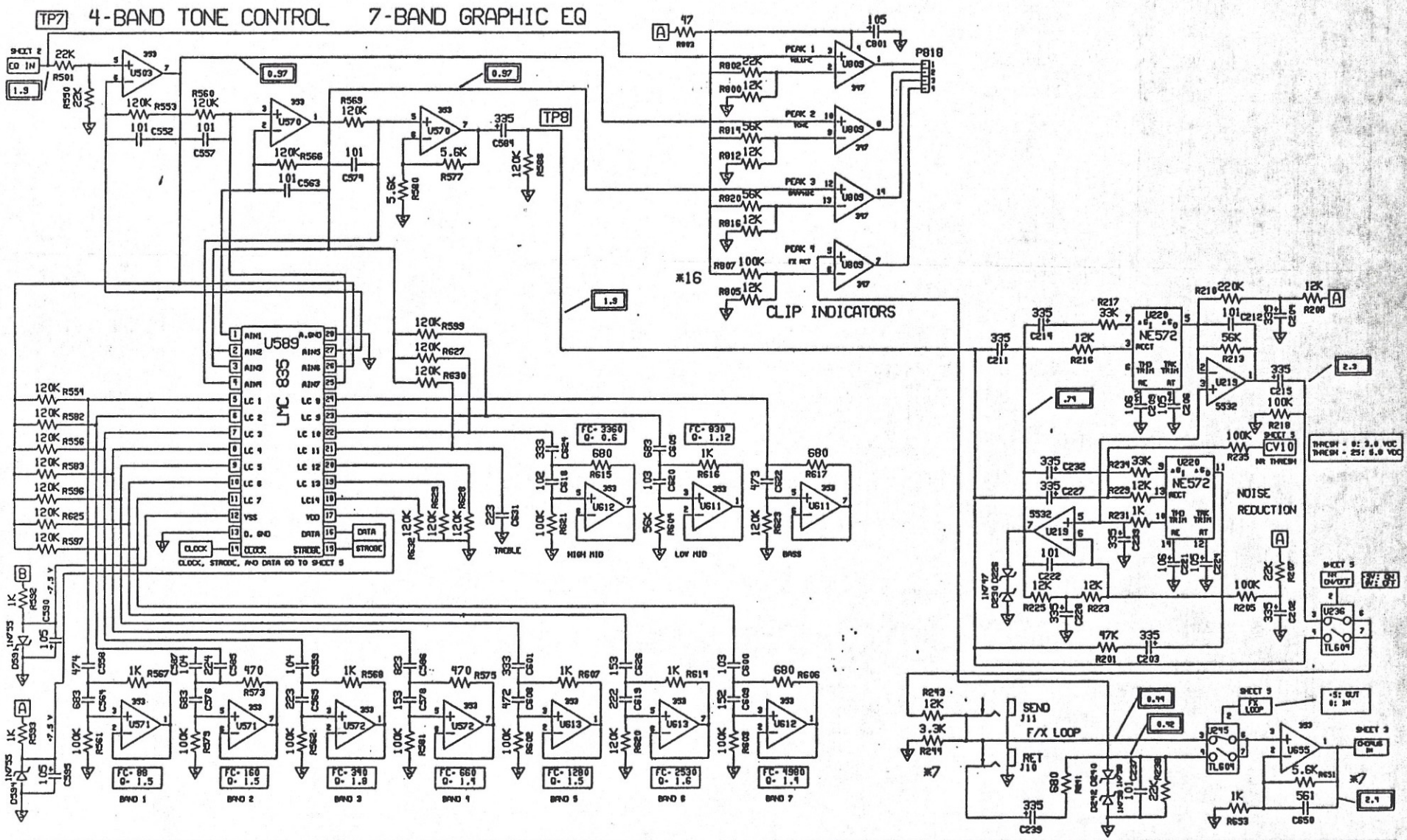

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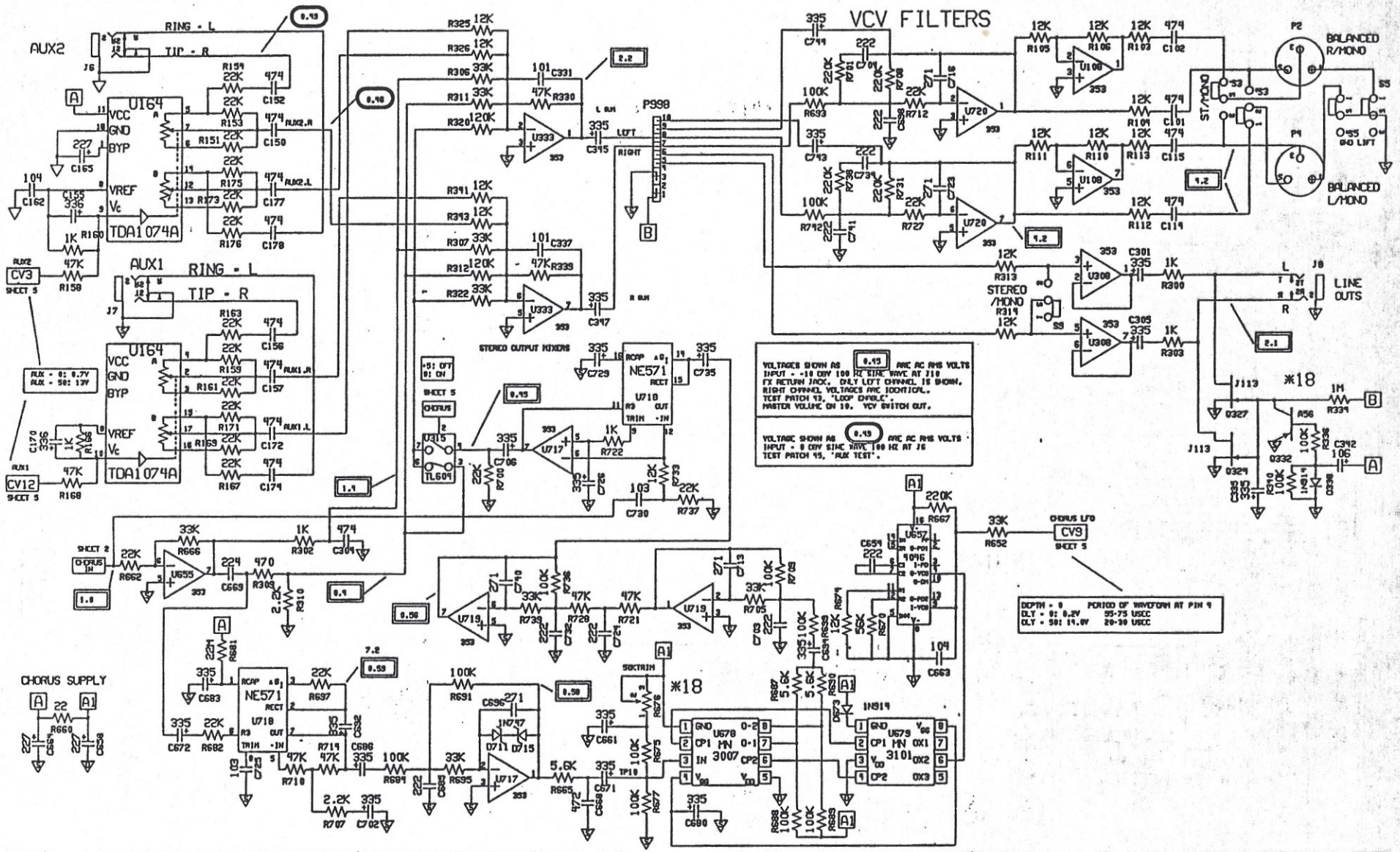

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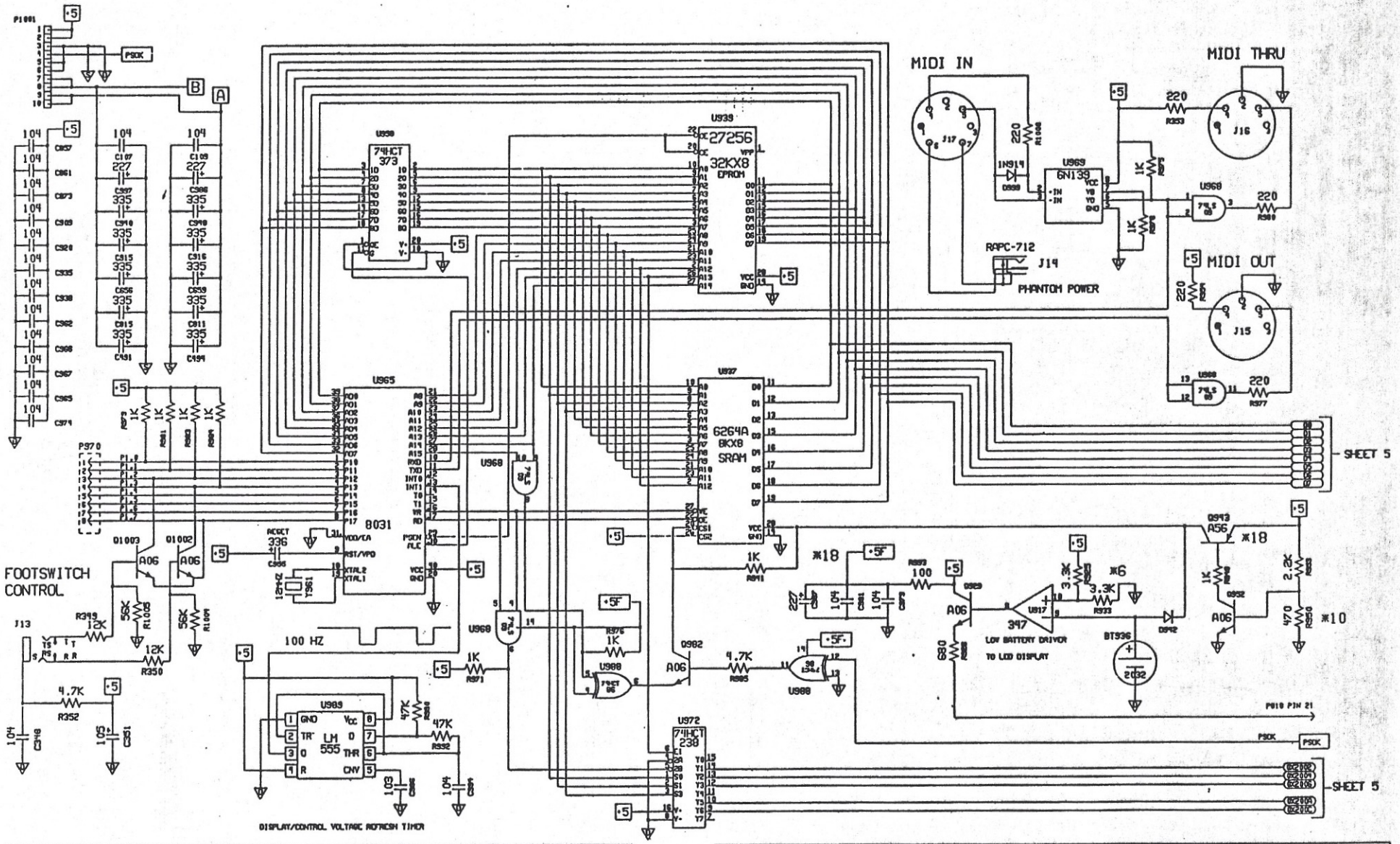

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GALLIEN-KRUEGER	MODEL #: 100MPL	DATE: 8/26/91	DESCRIPTION: MICROPROCESSOR		
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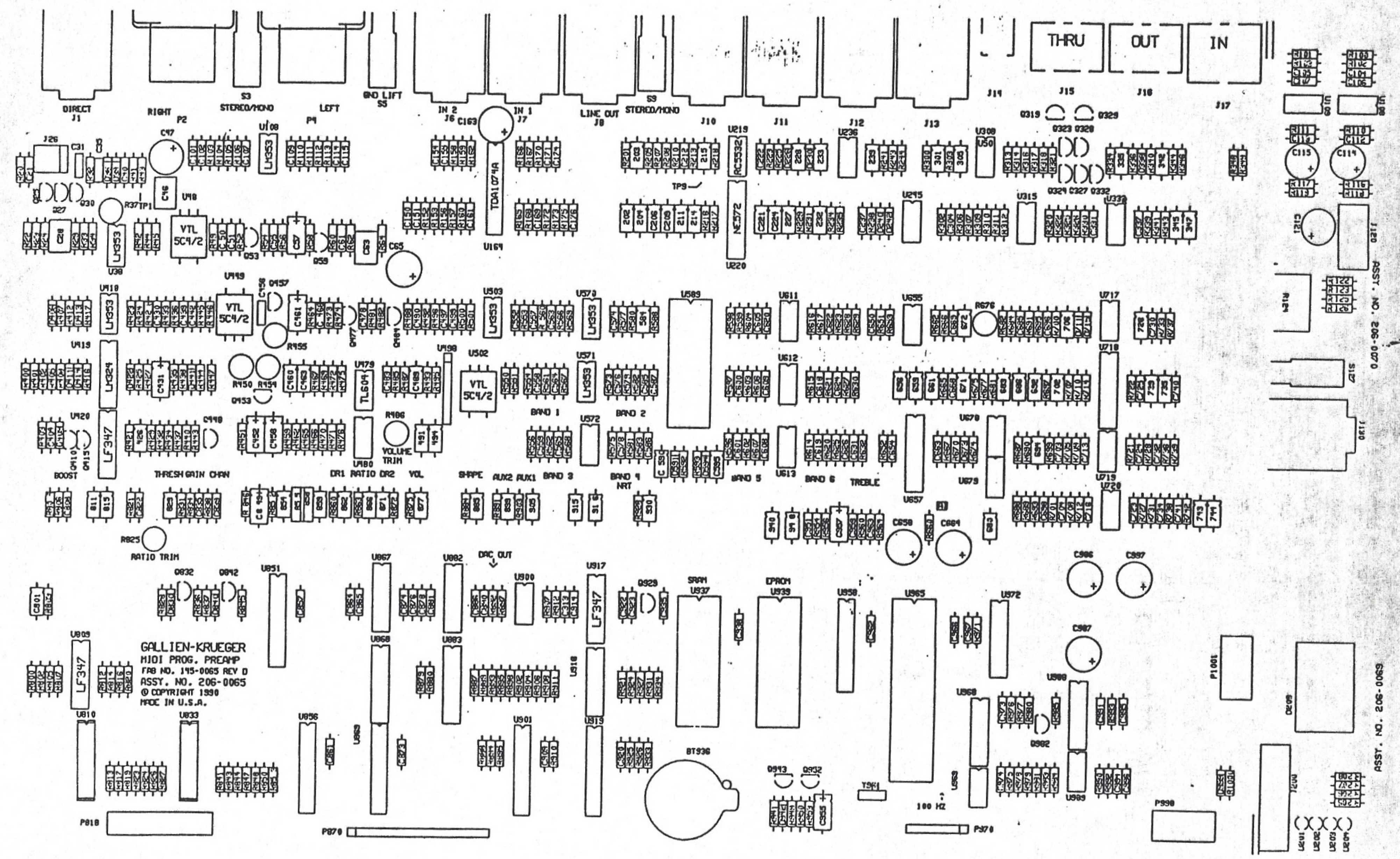
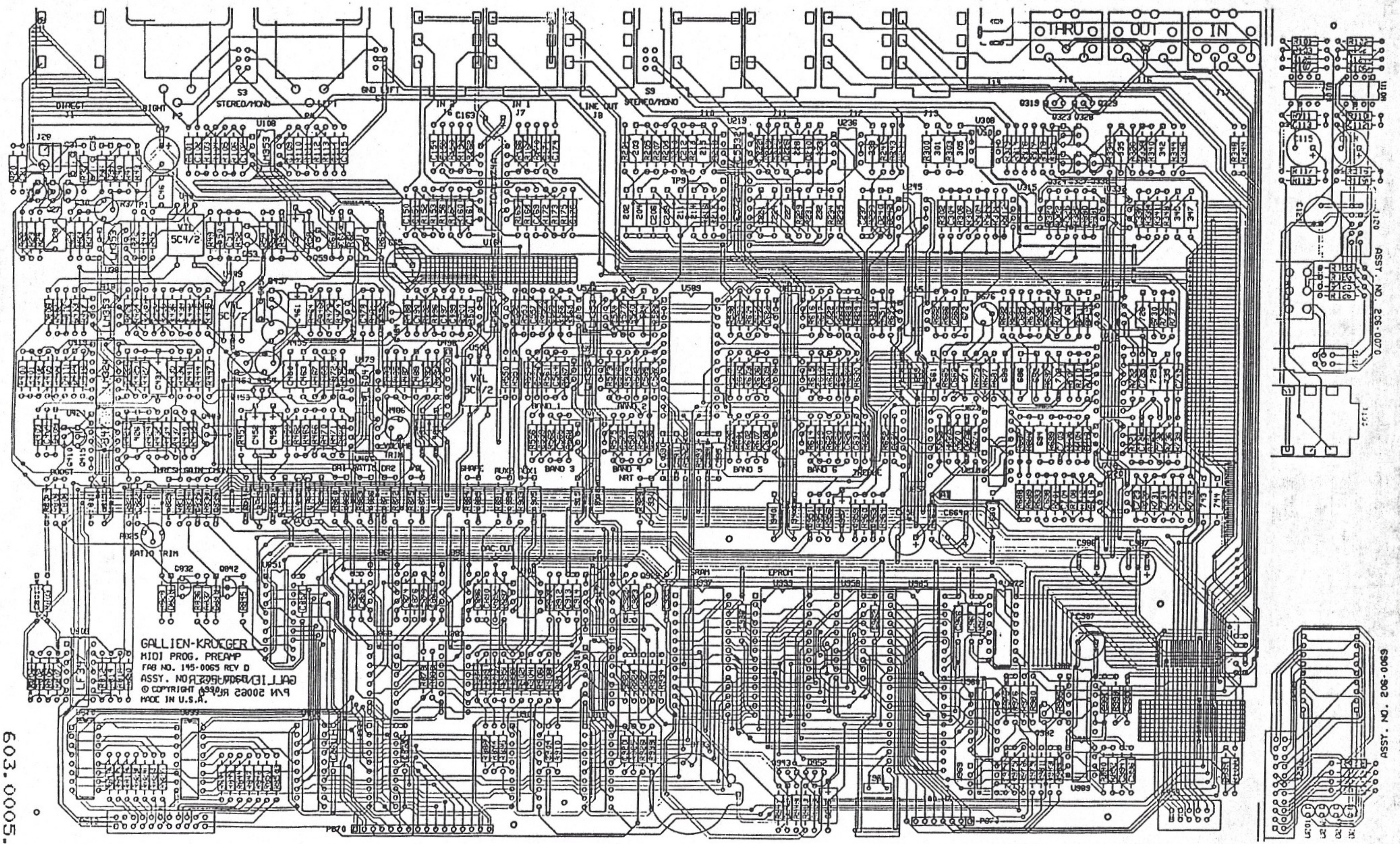

THRU
OUT
IN
DIRECT J1
RIGHT P2
S3 STEREO/MONO
LEFT P4
GND LIFT S5
IN 2 J6
IN 1 J7
LINE OUT J8
S9 STEREO/MONO
J10
J11
J12
J13
J14
J15
J16
J17
TDA1074A
RC5532
NE572
VTL 5C4/2
LM353
LM324
LF347
TL604
BOOST
RATIO TRIM
VOLUME TRIM
THRESH GAIN CHAN
DR1 RATIO DR2
VOL
SHAPE
AUX2 AUX1
BAND 1
BAND 2
BAND 3
BAND 4 NRT
BAND 5
BAND 6
TREBLE
DAC OUT
SRAM U937
EPROM U939
BT936
100 HZ
GALLIEN-KRUEGER
MIDI PROG. PREAMP
FAB NO. 145-0065 REV D
ASSY. NO. 206-0065
© COPYRIGHT 1990
MADE IN U.S.A.
ASSY. NO. 206-0070
ASSY. NO. 206-0069


GALLIEN-KRUEGER
MIDI PROG. PREAMP
FAB NO. 145-0065 REV D
© COPYRIGHT 1990
MADE IN U.S.A.
THRU
OUT
IN
STEREO/MONO
DIRECT
RIGHT
LEFT
LINE OUT
RATIO TRIM
SRAM
EPROM
BAND 1
BAND 2
BAND 3
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BAND 5
BAND 6
TREBLE
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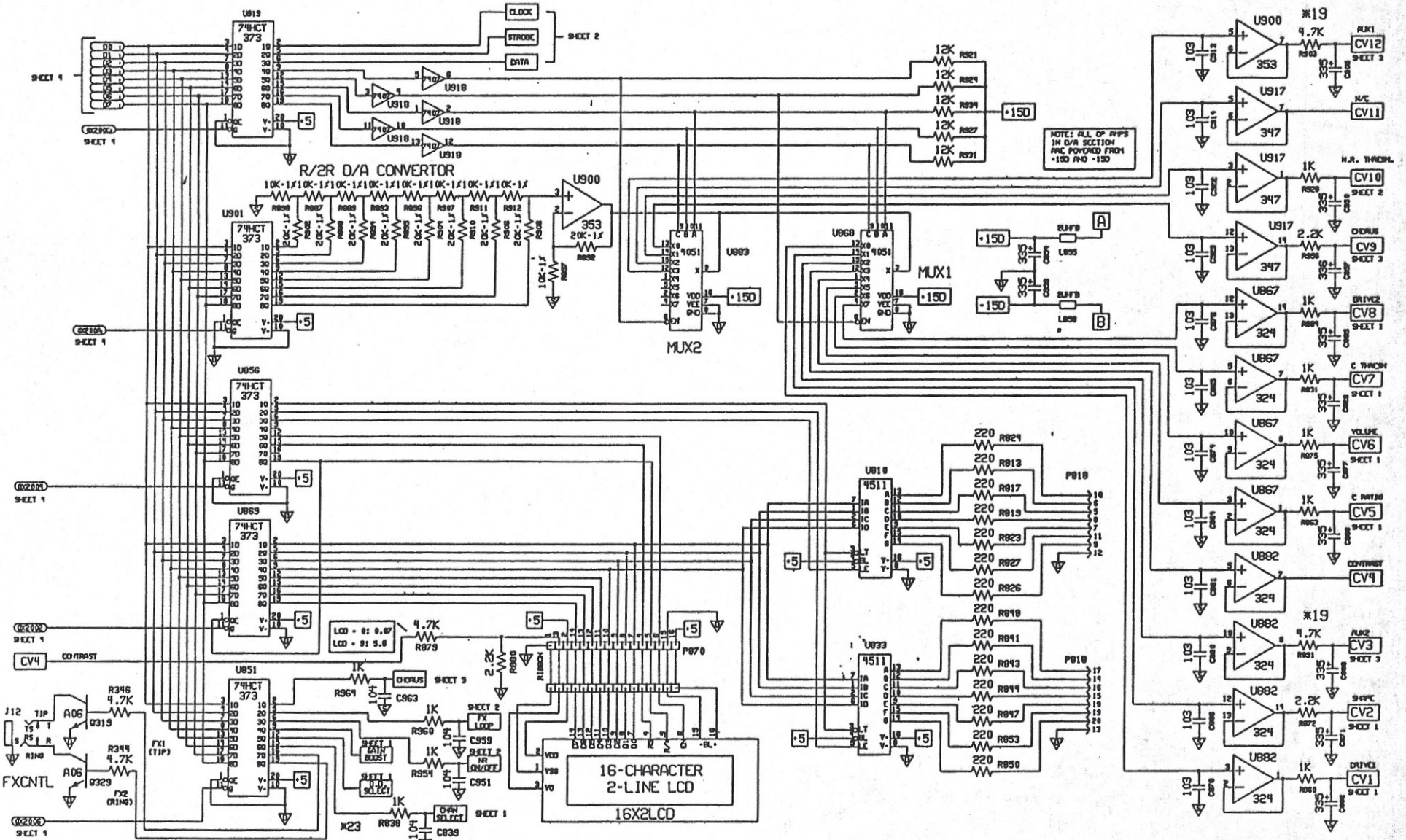
ASSY. NO. 206-0070
ASSY. NO. 206-0069

603.0005.5.10



PCO#	DATE	FIRST SN	PCO#	DATE	FIRST SN	PCO#	DATE	FIRST SN	PCO#	DATE	FIRST SN

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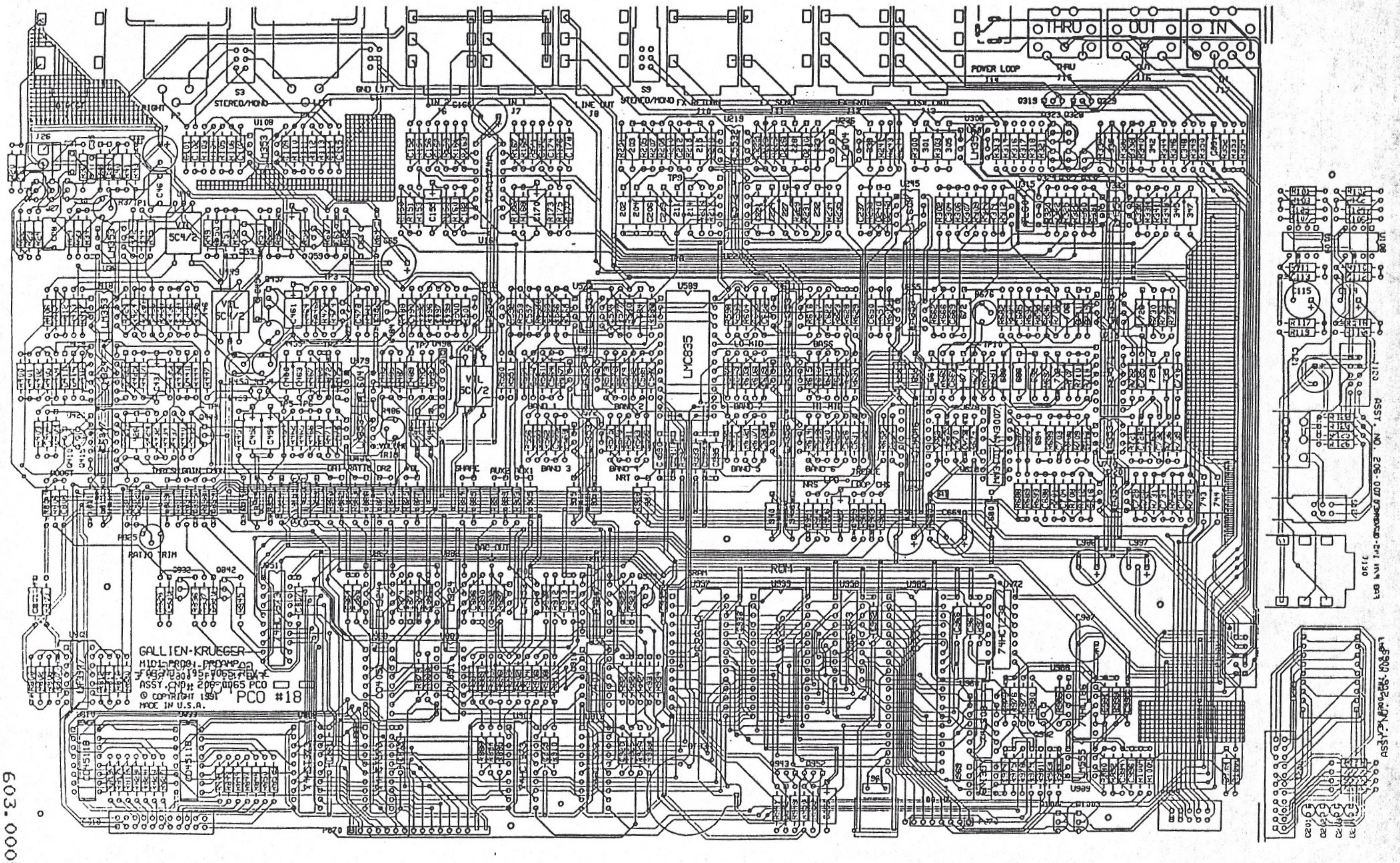
603.0005.4.44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OUT
IN
POWER LOOP
STEREO/MONO
GND LIFT
LINE OUT
FX RETURN
LMC835
LO MID
BASS
BAND 1
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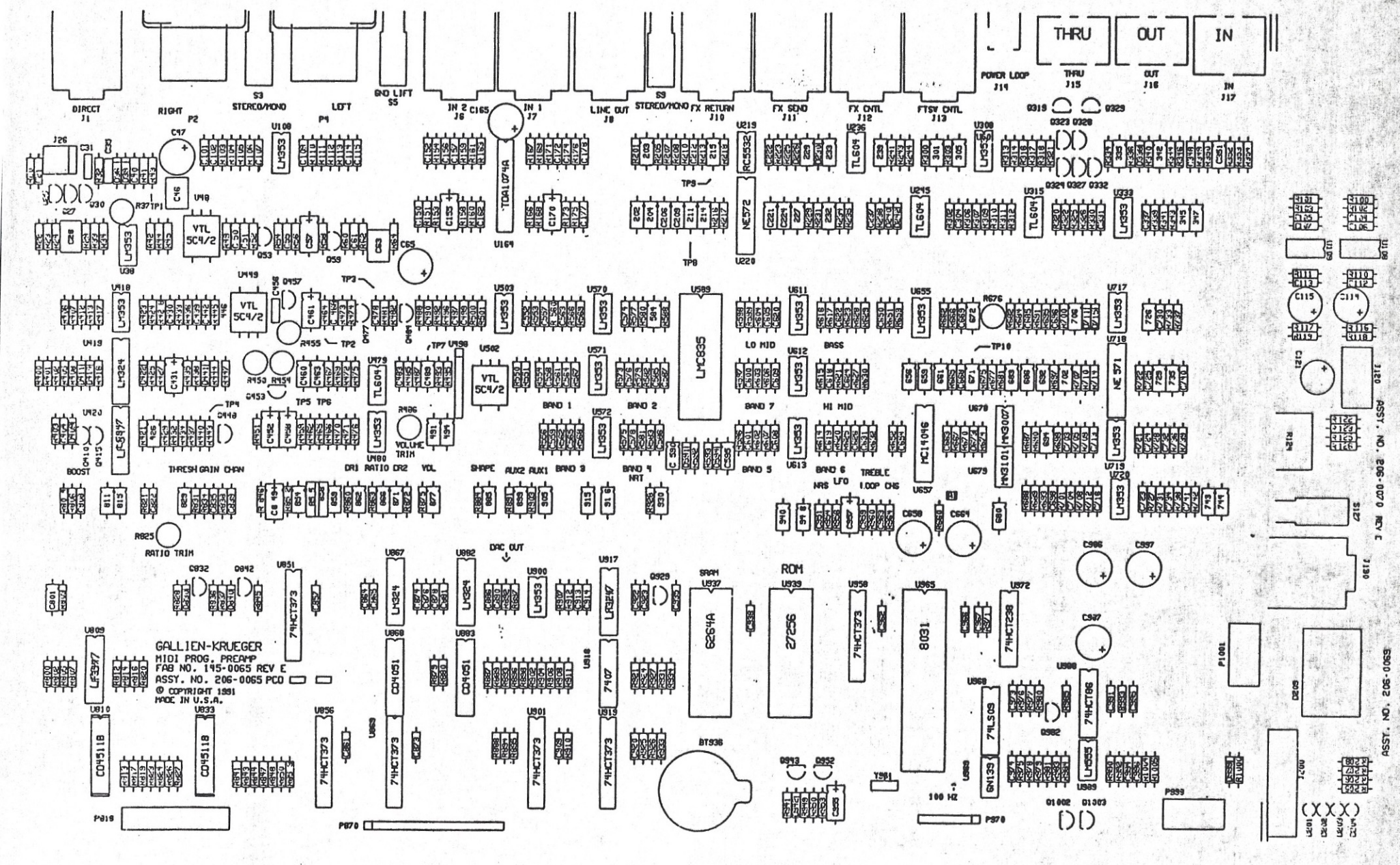
BAND 3
BAND 4
BAND 5
BAND 6
TREBLE
RATIO TRIM
ROM
SRAM
GALLIEN-KRUEGER
ASSY. NO. 206-0065 PCO
© COPYRIGHT 1991
MADE IN U.S.A.
PCO #18

603.0005.5.11


DIRECT J1
RIGHT P2
S3 STEREO/MONO
LEFT P4
GND LIFT S5
IN 2 J6
IN 1 J7
LINE OUT J8
S3 STEREO/MONO
FX RETURN J10
FX SEND J11
FX CNTL J12
FTSW CNTL J13
POWER LOOP J14
THRU J15
OUT J16
IN J17
GALLIEN-KRUEGER
MIDI PROG. PREAMP
FAB NO. 145-0065 REV E
ASSY. NO. 206-0065 PCO
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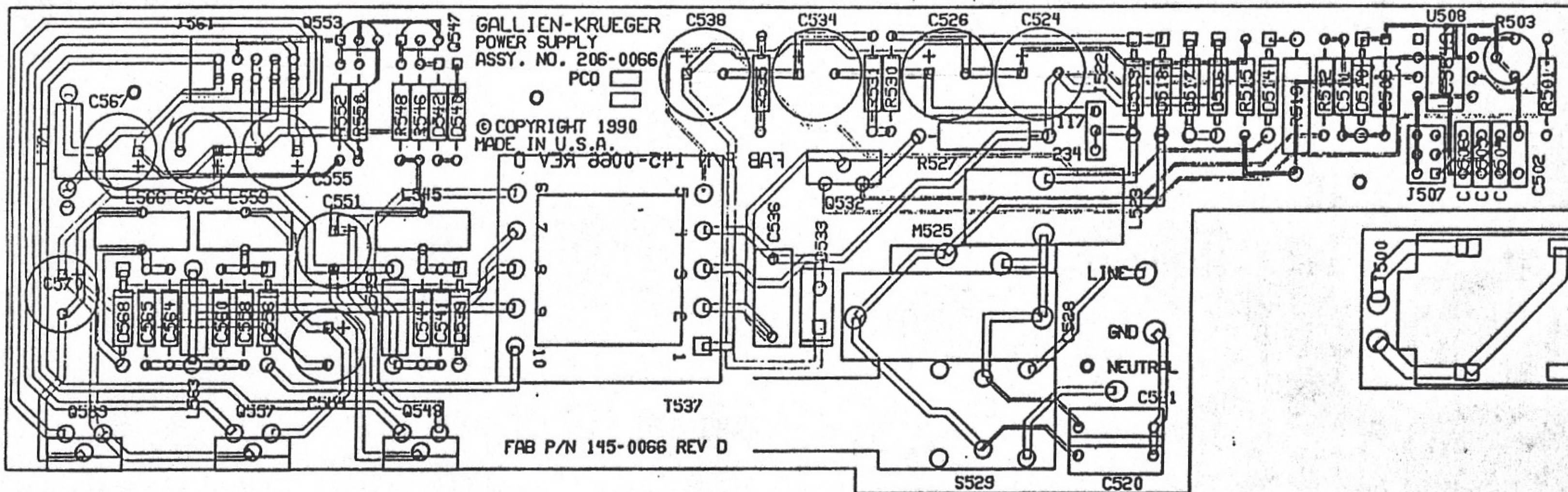
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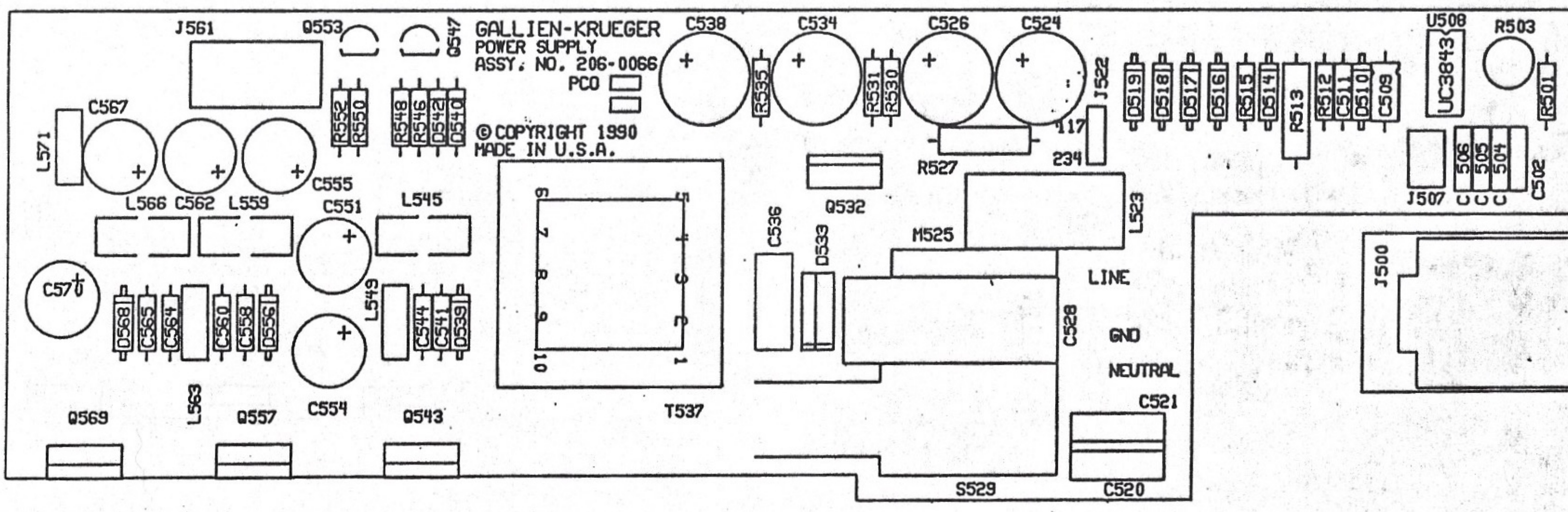
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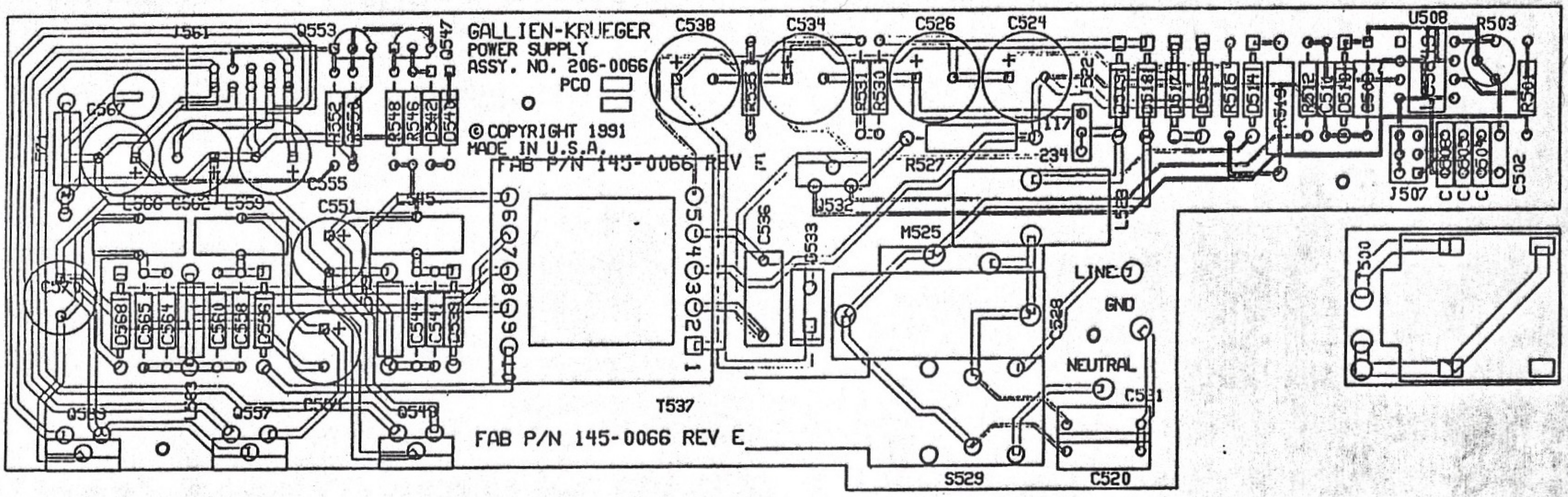
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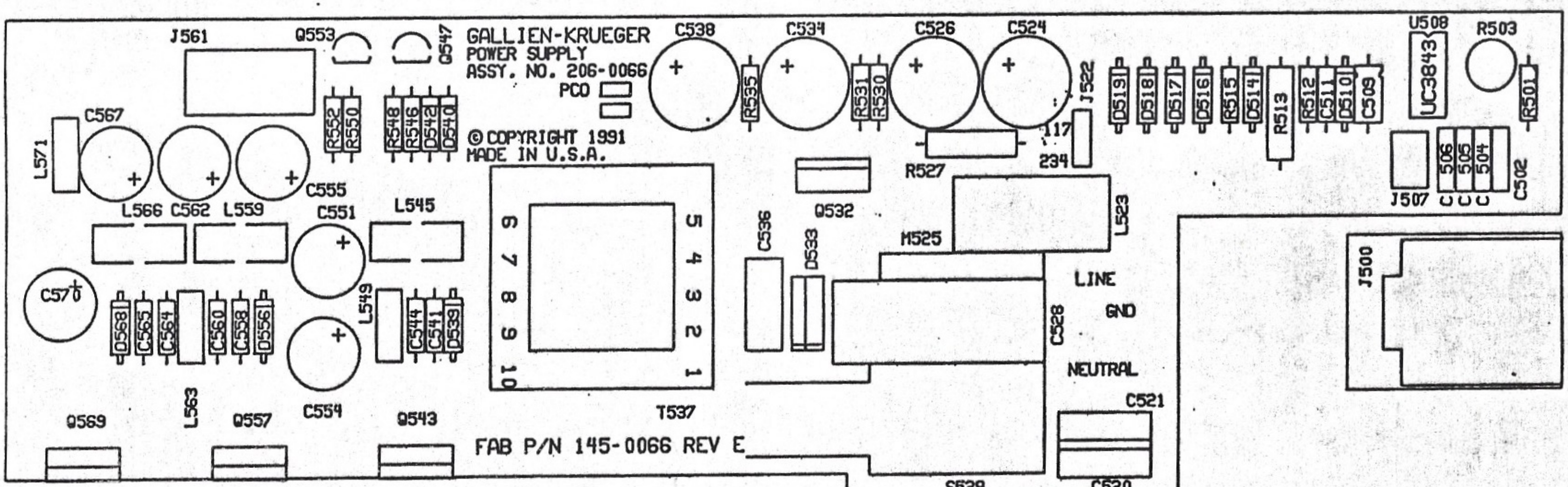
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